

Advance Registration Form

February 22-25, 2010

To register, mail or fax this form with payment to:

Design & Verification Conference & Exhibition

Attn: Registration Desk
1721 Boxelder St., Ste. 107
Louisville, CO 80027 USA



All registrations received after January 29, 2010, will be charged the "at-conference" rate. Payment with registration must be made in US dollars drawn from a US bank and made payable to: Design & Verification Conference & Exhibition. If payment is received from a non-US bank, attendees will be charged a collection fee of \$45.00. TELEPHONE REGISTRATIONS WILL NOT BE ACCEPTED! Fax registrations accepted with credit card payment only. FAX Number: (303) 530-4334

1 TYPE OR PRINT ATTENDEE INFORMATION

First Name _____ Last Name _____ Company _____
Address _____
City _____ State _____ Zip _____ Country _____
Phone _____ Fax _____ Email _____

2 CONFERENCE TUTORIALS – MONDAY AND TUESDAY, FEBRUARY 22 - 23

(Please select any tutorial(s) you plan to attend.) Monday and Tuesday Sponsored Tutorials are included in Full Conference, Student Full Conference and One-Day Only Registration. Includes access to one tutorial on Monday afternoon; and two tutorials on Tuesday one morning and one afternoon tutorial. Registrants will receive the (3) tutorial notes to their selected tutorials only. DVCon tutorial notes are not available for sale. Exhibit Only can purchase tutorials for \$60.00 per tutorial.

Monday, February 22

- _____ 1) Advanced Verification Techniques Using VMM,
sponsored by: Doulos (1:30-5:00pm)
- _____ 2) The OSCI TLM-2.0 Standard and Synthesis Subset Using VMM,
sponsored by: OSCI (1:30-5:00pm)
- _____ 3) Achieving Productivity Gains Through Formal Assertion-Based Verification (ABV)
sponsored by: OpenSpin (1:30-5:00pm)

Tuesday, February 23

- _____ 4) Experience with VIP Interoperability Best Practices
sponsored by: Accellera (8:30am-12:00pm)
- _____ 5) Rapid Prototyping Made Easy: A Hands-On Tutorial
sponsored by: Synopsys (8:30am-12:00pm)
- _____ 6) OVM Advanced Applications
sponsored by: Cadence (1:30pm-5:00pm)
- _____ 7) A Step-By-Step Guide to Advanced Verification
sponsored by: Mentor Graphics (1:30pm-5:00pm)

3 REGISTRATION FEES

STATUS	Before Jan. 29, 2010	After Jan. 29, 2010
_____ Full Conference	\$485	\$565
_____ Student	\$280	\$300
_____ One-Day Only	\$320	\$350
_____ Exhibit-Only Pass circle day- _____ Weds. _____ Thurs.	FREE	FREE
_____ Exhibit-Only w/Monday & or Tuesday Tutorials _____ Mon Aft. _____ Tues Morn. _____ Tues Aft. _____	\$60/Tutorial \$50	\$60/Tutorial \$50
_____ Extra CD-Rom Proceedings		\$50

4 PAYMENT INFORMATION (required)

Registration Fees \$ _____	Credit Card: _____ VISA _____ MASTERCARD _____ AMERICAN EXP.
Proceedings \$ _____	Card # _____
Tutorial Fees \$ _____	Name _____ Exp. Date _____ Sec. Code _____
TOTAL COST \$ _____	Please print name as it appears on the credit card

No refunds will be made unless a written request for cancellation is received prior to January 29, 2010. All refunds are subject to a \$35.00 processing fee. Requests for refunds received after the January 29, 2010 postmark date will not be honored and all registration fees will be forfeited. *NO REGISTRATIONS WILL BE ACCEPTED POSTMARKED AFTER February 18, 2010, IN THE DVCON OFFICE. After February 18, 2010, there will be at-conference registration only.

5 ATTENDEE SURVEY

1. Which is your primary design language? (Pick one)
____ 101) Verilog
____ 102) VHDL
____ 103) C/C++
____ 104) SystemC
____ 105) SystemVerilog
____ 106) Other _____

2. Which primary verification language do you use? (Pick one)
____ 201) C/C++
____ 202) e
____ 203) OpenVera
____ 204) Verilog
____ 205) VHDL
____ 206) SystemC
____ 207) SystemVerilog
____ 208) Other _____

3. Which primary verification language do you plan to use for your next design? (Pick one)
____ 301) C/C++
____ 302) e
____ 303) OpenVera
____ 304) Verilog
____ 305) VHDL
____ 306) SystemC
____ 307) SystemVerilog
____ 308) Other _____

4. Which primary property specification (assertion-based verification) language do you use?
____ 401) Verilog
____ 402) VHDL
____ 403) PSL
____ 404) System Verilog (SVA)
____ 405) Other _____

5. What area(s) are you focused on? (Check all that apply)
____ 501) Systems Design
____ 502) Standard ICs
____ 503) ASICs
____ 504) DSP Design
____ 505) Microprocessor/Multicontroller Design
____ 506) FPGAs & PLDs
____ 507) Multichip Modules
____ 508) PCBs
____ 509) Library Development
____ 510) Analog/Mixed Signal
____ 511) EDA Tools
____ 512) Verification
____ 513) SoCs
____ 514) Other _____

6. What on-chip buses do you plan to use in the next 12 months?
____ 601) AMBA 2.0 AHB/APB
____ 602) AMBA 3 AXI
____ 603) OCP 2.0
____ 604) OCP 2.1
____ 605) CoreConnect
____ 606) Others/Proprietary _____
____ 607) None

7. What interface standards do you expect to use in the next 12 months?
____ 701) PCI Express 1.1
____ 702) PCI Express 2.0
____ 703) USB 2.0/OTG
____ 704) Serial ATA
____ 705) 10G Ethernet
____ 706) 10/100/1G Ethernet
____ 707) Wireless USB
____ 708) PCI/PCI-X
____ 709) CE-ATA
____ 710) None

8. What is the size in gates of your current/last design? (Pick one)
____ 801) Not Applicable
____ 802) <1M
____ 803) 1-3M
____ 804) 3-5M
____ 805) 5-10M
____ 806) 10-50M
____ 807) >50M

9. How many clock domains do your designs average? (Pick one)
____ 901) 1
____ 902) 2
____ 903) 2-5
____ 904) 5-10
____ 905) 10-20
____ 906) >20
____ 907) Not Applicable

10. What is your number one design constraint? (Pick one)
____ 1001) Low power
____ 1002) Size/density
____ 1003) Performance/throughput
____ 1004) Other _____

11. What are the two main reasons for your attendance at DVCon? (Check all that apply)
____ 1101) Learn new techniques to improve your design process
____ 1102) Learn new methodologies to improve your verification process
____ 1103) Learn about new developments in design tools
____ 1104) Meet and network with other engineers in the industry
____ 1105) Learn about the industry in general
____ 1201) Senior Management
____ 1202) Engineering Management
____ 1203) Design Engineer
____ 1204) System Architecture
____ 1205) Application Engineer
____ 1206) Marketing
____ 1207) Technical Marketing
____ 1208) Product Marketing
____ 1209) Sales
____ 1210) Research / Academic
____ 1211) CAD
____ 1212) Verification Engineer
____ 1213) Other _____

DVCon makes a list of attendees available to exhibitors. Check here if you do not want to be included on this list _____