

Accellera Approves New Version of Electronic Design System Modeling Standard

Standard Co-Emulation Modeling Interface (SCE-MI) Improves Model Portability and Performance for Faster Design Verification

Napa, California, USA, 27 January 2011 -- Accellera, an Electronic Design Automation (EDA) standards organization, announced today that its Board of Directors approved a new version of Accellera's **Standard Co-Emulation Modeling Interface** (SCE-MI) specification as a new Accellera verification standard. Version 2.1 speeds up electronic design verification since it allows a model developed for simulation to run in an emulation environment and vice versa. Version 2.1 has added support for a subset of the [SystemVerilog Direct Programming Interface](#) (DPI) and built a streaming, variable length messaging system on top of this, which reduces the number of synchronizations when compared to other available methodologies. [Click here to download the standard.](#)

“Accellera standards improve the electronic design experience for the semiconductor industry,” remarked Shishpal Rawat, Accellera Chair. “We created this standard to alleviate one of the most critical bottlenecks in the electronic design cycle: verification. Given the reality of continually increasing design size and complexity, significant verification is enabled by SCE-MI as it allows simulation and emulation to be more interoperable.”

“EDA suppliers are working to bring new SCE-MI 2.1 capabilities to their customers as quickly as possible, and our committee will continue to add features that address portability, performance and ease of use,” said Brian Bailey, Interface Technical Committee (ITC) committee chair.

A previous version of the standard, SCE-MI 2.0, was approved by the Accellera Board in [May 2007](#). The SCE-MI standard was first created and is being continually improved by Accellera's Interface Technical Committee (ITC).

The SCE-MI standard provides an easy way to connect and migrate transaction models between simulation, emulation and rapid prototyping environments. With it, design and verification teams can realize improved electronic design productivity. Model portability enhancements for transaction-level verification on heterogeneous platforms make it worthwhile for more developers

to support SCI-MI-based models and for more users to make it part of their verification methodology.

More about the SCE-MI 2.1 Standard

The ITC committee's goal is to reduce the effort necessary to get a system into an emulation or prototyping environment for verification. In order to do that the models at the boundaries - transactors - have to be as similar as possible to those that would have been used in a simulation environment. To do this, SCE-MI 2.1 incorporates a subset of the SystemVerilog DPI which is available in most simulators. On top of this, a new transaction pipe interface has been defined, which adds support for variable length messaging and streaming data. Efficiency across the interface is paramount to getting the best possible utilization of the hardware, and these new capabilities add more control over when and how traffic moves around the system.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA and IP standards that lower the cost to design commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are transferred to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org. For membership information, please email membership@accellera.org.

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