



## Accellera Approves Universal Verification Methodology (UVM™) Standard

*Open-Source SystemVerilog base class library implementation and User Guide accompanies the UVM Class Reference Manual; Workshop set for Monday, Feb. 28 at DVCon*

NAPA, Calif., February 21, 2011 — [Accellera](#), the electronics industry organization focused on the creation and adoption of Electronic Design Automation (EDA) standards and Intellectual Property (IP) standards, approved version 1.0 of its **Universal Verification Methodology (UVM) standard**.

This standard, developed by Accellera's [Verification IP \(VIP\) Technical Subcommittee \(TSC\)](#), is available as a Class Reference Manual accompanied by an open-source SystemVerilog base class library implementation and a User Guide. The UVM standard establishes a methodology to improve design and verification efficiency, verification data portability and tool, and VIP interoperability.

The UVM Class Reference Manual is available for no cost at [www.accellera.org](http://www.accellera.org).

To read what the UVM community of producers and consumers are saying about the standard, [please click here](#).

“UVM puts in place a single, open standard to advance verification productivity within design teams and across multi-company design and verification collaborative efforts,” said Shishpal Rawat, Accellera chair. “In addition to the Class Reference Manual, a User Guide and open-source reference implementation are available to accelerate industry adoption.”

“This is a significant accomplishment because the new features were complex and required considerable effort to build from a full list of requirements,” said Hillel Miller, co-chair, Accellera’s VIP TSC. “The committee reconciled the requirements list, agreed to a specification, implemented them and tested the results in an effort that coordinated hundreds of people across several continents.”

“This was more than just a standards effort, it was a major software development project in a committee environment involving 18 leading verification companies,” said Tom Alsop, co-chair, Accellera’s VIP TSC. “Every major feature requested by the verification community was

implemented, including two new features built by the committee – a command line interface and Resource Manager.”

UVM 1.0 leverages features from the baseline UVM 1.0 Early Adopter (EA) release, a direct derivative of the Open Verification Methodology (OVM). This allowed the Accellera VIP TSC to focus on adding features found in other common methodologies to satisfy the agreed functional requirements to shorten the standards development cycle.

UVM 1.0 fully qualifies the baseline features, corrects most of the known bugs and implements enhancement requests. Major new features include a Phasing mechanism, a Register Package (derived from Verification Methodology Manual (VMM) technology) and support for the [Open SystemC Initiative](#)'s (OSCI) Transaction Level Modeling-2.0 (TLM-2.0) standard to model component transaction connectivity and communication. The Resource Manager is an upgrade to the configuration mechanism that makes it more general and includes a standardized command line interface. Additional new features include callbacks, message catching and functionality in the objection mechanism to manage end of test.

### **UVM at DVCon**

At its [Design Verification Conference and Exposition](#) (DVCon), Accellera is sponsoring a [workshop to unveil UVM on Monday, February 28, 2011](#). The day-long workshop features a comprehensive tutorial to educate verification engineers of all skill levels on the features of the industry's first open-source methodology fully supported and endorsed by all major EDA vendors and many end-user and consulting companies, both large and small.

The morning session will introduce many of the fundamental concepts in UVM. This will be followed by a walk-through of the key features needed to build a verification environment including stimulus generation and test shutdown. A discussion on the TLM communication mechanisms that leverage the OSCI TLM1 and TLM2 concepts will conclude the morning session.

A joint luncheon and Town Hall meeting with OSCI will allow participants to exchange additional collaboration ideas.

The afternoon session focuses on UVM component and environment control, including run-time phase management. There is an afternoon break with poster sessions from members of the UVM community.

A discussion of the UVM register package, including how to create and manage stimulus and checking at the register level follows the break. The session concludes with a review to show how the pieces all fit together.

### **About Accellera**

[Accellera](#) provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA and IP standards that lower the cost to design commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are transferred to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit [www.accellera.org](http://www.accellera.org). For membership information, please email [membership@accellera.org](mailto:membership@accellera.org).

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