



**2009 Design and Verification Conference
Attendee Questionnaire Results
Based on 665 responses**

	Count	Percents
Which is your primary design language? (Pick one)		
Verilog	343	53%
VHDL	61	9%
C/C++	82	13%
SystemC	42	6%
SystemVerilog	125	19%
	653	100%
Which primary verification language do you currently use? (pick one)		
C/C++	104	16%
e	27	4%
OpenVera	25	4%
Verilog	160	25%
VHDL	39	6%
SystemC	57	9%
System Verilog	238	37%
	650	100%
Which primary verification language do you plan to use for your next design? (Pick one)		
C/C++	91	14%
e	24	4%
OpenVera	14	2%
Verilog	114	18%
VHDL	31	5%
SystemC	66	10%
SystemVerilog	310	48%
	650	100%
Which primary property specification (assertion-based verification) language do you use or plan to use?		
Verilog	188	31%
VHDL	48	8%
PSL	48	8%
SystemVerilog (SVA)	328	54%
	612	100%
What design area(s) are you focused on? (Check all that apply)		
Systems Design	198	11%
Standard ICs	63	4%
ASICs	299	17%
DSP Design	77	4%
Microprocessor/Microcontroller Design	120	7%
FPGAs & PLDs	195	11%
Multi-Chip Modules	43	2%
PCBs	48	3%
Library Development	36	2%
Analog/Mixed Signal	62	3%
EDA Tools	229	13%
Verification	259	14%
SOCs	163	9%
	1792	100%
What on-chip buses do you intend to use in the next 12 months?		
AMBA 2.0 AHB/APB	167	19%
AMBA 3 AXI	133	15%
OCP 2.0	47	5%
OCP 2.1	58	7%
CoreConnect	36	4%
Others/Proprietary	161	18%
None	288	32%
	890	100%

	Count	Percents
What standard interface do you expect to use in the next 12 months?		
PCI Express 1.1	83	7%
PCI Express 2.0	218	18%
USB 2.0/OTG	141	11%
Serial ATA	98	8%
10G Ethernet	115	9%
10/100/1G Ethernet	133	11%
Wireless USB	67	5%
PCI/PCI-X	78	6%
CE-ATA	13	1%
None	292	24%
	1238	100%
What is the size in gates of your current/last design? (Pick one)		
Not Applicable	246	36%
< 1M	69	10%
1 - 3M	54	8%
3 - 5M	57	8%
5 - 10M	90	13%
10M - 50M	104	15%
>50M	54	8%
	674	100%
How many clock domains do your designs average?		
1	90	14%
2	67	11%
2 - 5	216	35%
5 - 10	138	22%
10 - 20	57	9%
>20	58	9%
	626	100%
What is your number one design constraint?		
Low power	244	39%
Size/density	91	15%
Performance/throughput	286	46%
	621	100%
What are the two main reasons for your attendance at DVC on?		
Learn new techniques to improve your design process	202	16%
Learn new methodologies to improve your verification process	292	23%
Learn about new developments in design tools	259	20%
Meet and network with other engineers in the industry	297	23%
Learn about industry in general	221	17%
	1271	100%
Which category most closely describes your job description? (Pick one)		
Senior Management	120	18%
Engineering Management	110	16%
Design Engineer	122	18%
System Architecture	35	5%
Marketing & Sales	117	17%
Research/Academic	19	3%
CAD	38	6%
Verification Engineer	117	17%
	678	100%
DVC on provides an email list of attendees to exhibitors. If you DO NOT want to receive this correspondence check unsubscribe below.		
Unsubscribe	279	