

Registration Form

February 27 - March 1, 2012

To register, mail or fax this form with payment to:

Design & Verification Conference & Exhibition
Attn: Registration Desk
1721 Boxelder St., Ste. 107
Louisville, CO 80027 USA



All registrations received after January 27, 2012, will be charged the "at-conference" rate. Payment with registration must be made in US dollars drawn from a US bank and made payable to: Design & Verification Conference & Exhibition. If payment is received from a non-US bank, attendees will be charged a collection fee of \$45.00. TELEPHONE REGISTRATIONS WILL NOT BE ACCEPTED! Fax registrations accepted with credit card payment only. FAX Number: (303) 530-4334

1 TYPE OR PRINT ATTENDEE INFORMATION

First Name _____ Last Name _____ Company _____
Address _____
City _____ State _____ Zip _____ Country _____
Phone _____ Fax _____ Email _____

2 CONFERENCE TUTORIALS – MONDAY AND THURSDAY, FEBRUARY 27 AND MARCH 1

Monday, February 27

- 1) An Introduction to IEEE P1666-2011, the New SystemC Standard (1:30pm-5:00pm) *Sponsored by: SystemC*
- 2) UVM: Ready, Set, Deploy! (8:30am-5:00pm)
- 3) An Introduction to the Unified Coverage Interoperability Standard (2:00am-3:00pm)
- 4) Verification and Automation improvement using IP-XACT (3:30pm-5:30pm)

Tutorials are offered on Monday and Thursday and require an additional fee. Coffee breaks and luncheon are included with your tutorial attendance. Registrants will receive the tutorial notes to the selected tutorials only. **DVCon tutorial notes are not available for sale. ** Conference + 8 Tutorials or the Eight Tutorial registration receive all the tutorial notes.

Thursday, March 1

- 5) Using "Apps" to Take Formal Analysis Mainstream (8:30am-12:00pm) *Sponsored by: Cadence*
- 6) Design & Verification of Platform-Based, Multi-Core SoCs (8:30am-12:00pm) *Sponsored by: Mentor Graphics*
- 7) Leveraging Formal Verification Throughout the Entire Design Cycle (1:30pm-5:00pm) *Sponsored by: Jasper*
- 8) New Levels of Verification IP Productivity for SOC Verification (1:30pm-5:00pm) *Sponsored by: Synopsys*

3 REGISTRATION FEES

Registration Option	Before Jan. 27, 2012	After Jan. 27, 2012
Conference + 8 Tutorials	\$650	\$665
Conference + 4 Tutorials	\$500	\$515
Conference Only	\$450	\$465
One-Day Only - Circle Day: Tuesday Wednesday	\$325	\$355
Student Conference Only	\$285	\$310
Exhibits Only	\$0	\$0
Tutorial Only	\$75	\$75
Tutorial Eight Package	\$360	\$360

4 PAYMENT INFORMATION (REQUIRED)

Registration Fees \$ _____
Tutorial Fees \$ _____
TOTAL COST \$ _____

Credit Card: _____ VISA _____ MASTERCARD _____ AMERICAN EXP. _____
Card # _____
Name _____ Exp. Date _____ Sec. Code _____
Please print name as it appears on the credit card
Signature _____

No refunds will be made unless a written request for cancellation is received prior to January 27, 2012. All refunds are subject to a \$35.00 processing fee. Requests for refunds received after the January 27, 2012 postmark date will not be honored and all registration fees will be forfeited.

*NO REGISTRATIONS WILL BE ACCEPTED POSTMARKED AFTER February 24, 2012, IN THE DVCON OFFICE. After February 24, 2012, there will be at-conference registration only.

5 ATTENDEE SURVEY

1. Which is your primary design language? (Pick one)
___101) Verilog
___102) VHDL
___103) C/C++
___104) SystemC
___105) SystemVerilog
___106) Other _____

2. Which primary verification language do you use? (Pick one)
___201) C/C++
___202) e
___203) OpenVera
___204) Verilog
___205) VHDL
___206) SystemC
___207) SystemVerilog
___208) Other _____

3. Which primary verification language do you plan to use for your next design? (Pick one)
___301) C/C++
___302) e
___303) OpenVera
___304) Verilog
___305) VHDL
___306) SystemC
___307) SystemVerilog
___308) Other _____

4. Which verification methodology is used by your functional verification team
___401) UVM
___402) OVM
___403) VMM
___404) eRM
___405) SystemC/TLM
___406) Home Grown
___407) Other _____
___408) I am not involved

5. Which primary property specification (assertion-based verification) language do you use?
___501) Verilog
___502) VHDL
___503) PSL
___504) System Verilog (SVA)
___505) Other _____

6. What area(s) are you focused on? (Check all that apply)
___601) Systems Design
___602) Standard ICS
___603) ASICs
___604) DSP Design
___605) Microprocessor/Multicontroller Design
___606) FPGAs & PLDs
___607) Multichip Modules
___608) PCBs
___609) Library Development
___610) Analog/Mixed Signal
___611) EDA Tools
___612) Verification
___613) SoCs
___614) Software/Embedded Software
___615) Other _____

7. What on-chip buses do you plan to use in the next 12 months?
___701) AMBA 2.0 AHB/APB
___702) AMBA 3 AXI
___703) OCP 2.0
___704) OCP 2.1
___705) CoreConnect
___706) Others/Proprietary _____
___707) None

8. What interface standards do you expect to use in the next 12 months?
___801) PCI Express 1.1
___802) PCI Express 2.0
___803) USB 2.0/OTG
___804) Serial ATA
___805) 10G Ethernet
___806) 10/100/1G Ethernet
___807) Wireless USB
___808) PCI/PCI-X
___809) CE-ATA
___810) None

9. What is the size in gates of your current/last design? (Pick one)
___901) Not Applicable
___902) <1M
___903) 1-3M
___904) 3-5M
___905) 5-10M
___906) 10-50M
___907) >50M

10. How many clock domains do your designs average? (Pick one)
___1001) 1
___1002) 2
___1003) 2-5
___1004) 5-10
___1005) 10-20
___1006) >20
___1007) Not Applicable

11. What is your number one design constraint? (Pick one)
___1101) Low power
___1102) Size/density
___1103) Performance/throughput
___1104) Other _____

12. What are the two main reasons for your attendance at DVCon? (Check all that apply)
___1201) Learn new techniques to improve your design process
___1202) Learn new methodologies to improve your verification process
___1203) Learn about new developments in design tools
___1204) Meet and network with other engineers in the industry
___1205) Learn about the industry in general

13. Which category most closely describes your job description? (Pick one)
___1301) Senior Management
___1302) Engineering Management
___1303) Design Engineer
___1304) System Architecture
___1305) Application Engineer
___1306) Marketing
___1307) Technical Marketing
___1308) Product Marketing
___1309) Sales
___1310) Research / Academic
___1311) CAD
___1312) Verification Engineer
___1313) Software Engineer
___1314) Other _____

DVCon makes a list of attendees available to exhibitors. Check here if you do not want to be included on this list _____