



DVCon

**design & verification
conference & exhibition**

February 21 - 23, 2007

DoubleTree Hotel • San Jose, CA

www.dvcon.org

sponsored by:



Final Program



Design and Verification Conference and Exhibition

Chair's Welcome

On behalf of the DVCon 2007 Steering and Program committees, we invite you to attend the Design & Verification Conference and Exhibition.

I would like to humbly dedicate this conference to the memory of Dr. Richard Newton. Without his work in the academic, technical, and business sectors of the EDA industry, most of the material presented and discussed at this and past DVCons would not exist, at least not in its present form. The EDA industry owes a significant debt to Richard's creativity, intuition, and practicality. I can only hope that DVCon conferences in the past, present and future will contribute to the growth of other leaders in the EDA industry.

Design and verification solutions must address different levels of abstraction concurrently, must deal successfully with hardware/software co-development, and must be multi-lingual because the application areas require the use of different languages. Designers and implementers will have to be familiar not only with those traditionally discussed in EDA circles like Verilog, VHDL, SystemC, C, and SystemVerilog, but also MATLAB, Esterel, and Rosetta. Innovation may not be enough; we need invention to put us

on pace with the continuing progress in electronic systems design and fabrication. The dedicated volunteers in the Steering and Program Committees have worked hard to assemble a conference that will stimulate the attendees in a number of areas from system design to physical implementation verification.

Although we must never forget the lessons we learned in the past, we must not be constrained by the way things have been done in the past. We must look at the present problems with a fresh approach, because the nature of the problems facing today's designers and verification engineers is different from what we have faced before. I trust that the material you will hear and see at DVCon 2007 will help in your endeavors.



Gabe Moretti
Gabe on EDA
2007 General Chair



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Sponsor

Accellera



To improve designers' productivity, the electronic design industry needs a methodology based on both worldwide standards and open interfaces. Accellera was formed in 2000 through the unification of Open Verilog International and VHDL International to focus on identifying new standards, development of standards and formats, and to foster the adoption of new methodologies.

Accellera's mission is to drive worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process. Its Board of Directors guides all the operations and activities of the organization, and is comprised of representatives from ASIC manufacturers, systems companies and design tool vendors.

Technical Committees

The Accellera Board of Directors established the Technical Committee (TC) to develop, update and extend hardware design language (HDL) standards. The TC is comprised of subcommittees that focus on the various standards under development, and report to the TC Chair. In addition, Accellera supports the activities of certain IEEE working groups and cooperates with other standards groups within the EDA industry.

Unified Power Format
Coverage API
Interface Technical Committee
Open Compression Interface

Open Verification Libraries
Verilog AMS
IEEE 1800 SystemVerilog
IEEE 1364 Verilog

IEEE P1850 PSL
IEEE 1076 VHDL

Membership

Accellera's members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, Accellera members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions which impact the EDA industry.

www.accelera.org

Wednesday, February 21, 2007

Morning Tutorials

9:00 am - 12:30 pm

see pages 6 & 7

Afternoon Tutorials

1:30 pm - 5:00 pm

see pages 8, 9 & 10

Tutorial 1 • Practical Deployment of Assertion-Based Verification and Formal Analysis

Sponsored by:

The logo for Cadence, featuring the word 'cadence' in a lowercase, sans-serif font with a horizontal line above the 'a'.

Tutorial 2 • Practical Applications of Mentor's Advanced Verification Methodology (AVM)

Sponsored by:

The logo for Mentor Graphics, featuring the words 'Mentor Graphics' in a bold, sans-serif font with a registered trademark symbol.

DVCon Exhibits (Cascade Ballroom)

4:00 pm - 7:00 pm

Tutorial 3 • Pragmatic Adoption of Verification Methodology Manual (VMM) for Re-usable Transaction-Based Testbenches in SystemVerilog

Sponsored by:

The logo for Synopsys, featuring the word 'SYNOPSYS' in a bold, uppercase, sans-serif font.

Tutorial 4 • Using Formal Verification to Attain Completeness and Correctness

Sponsored by:

Logos for Jasper Design Automation and Sun Microsystems. The Jasper logo includes the word 'JASPER' in a bold, uppercase font above 'design automation' in a smaller font. The Sun Microsystems logo includes the word 'Sun' in a stylized font above 'microsystems' in a smaller font.

Tutorial 5 • SystemC Transaction Level Modeling Standards and Methodology Guidelines

Sponsored by:

The logo for SystemC, featuring the word 'SYSTEMC' in a bold, uppercase, sans-serif font with a curved line above the letters.

DVCon Reception • 5:00 pm - 7:00 pm Sponsored by: **SYNOPSYS**



Design and Verification Conference and Exhibition

Wednesday, February 21, 2007

Tutorial sponsored by:

cādence™

Rm: Donner Ballroom • 9:00 am - 12:30 pm

Tutorial 1 • Practical Deployment of Assertion-Based Verification and Formal Analysis

Organizer: Michal Siwinski - *Cadence Design Systems, Inc.*

Presenter: Lovleen Bhatia - *Texas Instruments Inc.*

Erich Marschner - *Cadence Design Systems, Inc.*

Faisal Haque - *Verification Central*

Raghavan Menon - *Ingot Systems, Inc.*

Jon Michelson - *Verification Central*

Axel Scherer - *Cadence Design Systems, Inc.*

This half-day tutorial shows designers, verification engineers, and their management how to accelerate project schedules and improve product quality through the use of assertion-based verification (ABV) and formal analysis. Starting from the original verification plan, these techniques enable more thorough verification early in the development process, efficient reuse during the later stages of verification, and effective metrics to help determine when it is time to tape out.

The ABV methodology discussed in this tutorial spans block-level verification, chip-level simulation, and hardware acceleration/emulation. Attendees will learn how to apply the right verification technologies at the right phases of the development process to get the best results with the least amount of time and effort, thus providing the highest return on

investment. The focus is on practical deployment of these technologies, leveraging real-world experience to explain where they add value and where they are less productive.

The presenters include industry authorities on assertions and formal analysis, EDA experts who have helped thousands of engineers succeed with these techniques, and end users who discuss their experiences on large development projects. Attendees should have a basic understanding of assertions and how they are specified. Detailed knowledge of specific assertion formats or previous experience with formal analysis is not required to benefit from the techniques and applications covered in this tutorial.

Wednesday, February 21, 2007

Tutorial sponsored by:



Rm: Oak Ballroom • 9:00 am - 12:30 pm

Tutorial 2 • Practical Applications of Mentor's Advanced Verification Methodology (AVM)

Organizers: Tom Fitzpatrick - *Mentor Graphics Corp.*
Larry Toda - *Mentor Graphics Corp.*

Presenters: Tom Fitzpatrick - *Mentor Graphics Corp.*
Harry Foster - *Mentor Graphics Corp.*
Ambar Sarkar - *Paradigm Works*
John Aynsley - *Doulos Ltd.*

This in-depth, half-day tutorial covers using the Mentor Graphics Advanced Verification Methodology (AVM) to develop testbenches for real-world applications. The tutorial walks-through a detailed example of writing a testbench for a moderately complex design, the overall architecture, construction of individual verification components, and infrastructure to allow new scenarios to be generated with minimum additional coding.

While many engineers understand the concepts of new verification techniques, they may be unsure of how best to apply them to their particular project. Mentor's AVM was developed explicitly to help verification teams get past this "blank page" phase of the project by providing a library of modular, reusable transaction-level verification components to efficiently create transaction-level testbenches for today's advanced technologies: constrained-random stimulus, functional coverage, and assertions.

The tutorial begins with an overview of Transaction-Level Modeling, the AVM library, AVM components usage, the planning and analysis required to determine the optimal architecture for the verification of a router design (developed by Paradigm Works). Key aspects of the testbench: stimulus generation, assertions for functional coverage, and scoreboarding are discussed, plus a demonstration encapsulating the testbench for reusability and customization.

The next section covers writing effective assertions for simulation and formal verification, using assertions to gather transaction-level information, and how the AVM communicates information between modules and classes throughout the testbench.

The tutorial concludes with the AVM development process, the collaboration between Mentor Graphics, its partners, and customers. This discussion includes Dr. Sarkar on an overview of the SytemVerilog Frameworks, and Mr. Ansley on coverage-based methodology.

Tutorial sponsored by:

SYNOPSYS[®]**Rm: Donner Ballroom • 1:30 pm - 5:00 pm****Tutorial 3 • Pragmatic Adoption of Verification Methodology Manual (VMM) for Re-usable Transaction-Based Testbenches in SystemVerilog****Organizer:** Synopsys, Inc.**Presenters:** Srinivasan Venkataramanan - *Synopsys, Inc.*Ben Cohen - *Vhdlcohen Publishing*Ajeetha Kumari - *Contemporary Verification Consultants*

The Verification Methodology Manual (VMM) for SystemVerilog provides a proven, robust and scalable approach for building advanced verification environments. It captures years of industry best-practices for taking advantage of constrained-random, coverage-driven and assertion-based verification. However, absorbing all of this information can be a daunting task for engineers coming from a traditional directed-test verification background. This tutorial will present a pragmatic approach to VMM methodology adoption, guided by practical examples and straightforward explanations.

Attendees will learn how to build a VMM-compliant testbench. The tutorial will present by example the development of transactions and channels; the atomic transaction generator; the use of SystemVerilog interfaces; the command transactor and monitor;

the environment and testbench; the factory pattern. We will also explain how callbacks notifications can be used for the collection of coverage, for scoreboarding, and for the application of assertions that use class and interface variables. We will also explain by example the power of VMM for the definition of the scenario generators, and the application of schedulers and broadcasters.

Industry praise and support of the Verification Methodology Manual (VMM) for SystemVerilog, co-authored by ARM and Synopsys, has steadily increased since its introduction. Widespread adoption and user success has established the VMM as the industry's most robust and proven methodology for SystemVerilog. This tutorial is targeted at engineers and managers interested in adopting SystemVerilog for advanced functional verification.

Wednesday, February 21, 2007

Tutorial sponsored by:



Rm: Oak Ballroom • 1:30 pm - 5:00 pm

Tutorial 4 • Using Formal Verification to Attain Completeness and Correctness.

Organizer: Francine M. Bacchini - *Francine Bacchini, Inc.*

Presenters: Lawrence Loh - *Jasper Design Automation, Inc.*

Mercedes Tan - *Sun Microsystems*

Prosenjit Chatterjee - *NVIDIA*

Ideally suited for Hardware Design & Verification engineers, CAD and methodology engineers and managers, this verification planning tutorial will provide novice and advanced verification engineers the primary considerations involved in the establishment of a design, verification, optimization and debug methodology in today's changing verification landscape. Discussion includes: types of infrastructure and sets of resources available and necessary for successful methodology implementation.

The face of verification is changing. Simulation and random testbenches alone cannot ensure sufficient confidence in the design implementation. With increasing design size and complexity, come entirely new issues. Today's verification environment includes several new considerations: IP verification, integration of new verification technologies and new coverage concerns. Planning an effective verification flow around such diverse requirements is not easy - nor is Tracking the results over the verification lifetime.

Success in these areas is key to improving product quality and maintaining a tight development cycle to meet market opportunities. This tutorial begins with an overview of verification planning with formal integration, followed by a "how to" exposition on how to extract a meaningful verification plan from a specification by Jasper Design Automation. The growing size, complexity, and interactions within a single system require more comprehensive verification plans and the use of verification Intellectual Property (IP) to attain completeness and correctness in designs. Denali Software will discuss practical development and deployment tips for verification IP and demonstrate its use as a part of the overall verification plan. Issues and techniques for dealing with coverage concerns when integrating multiple verification technologies will be reviewed. Sun Microsystems will discuss the challenges faced with accurate coverage tracking and strategies for combing results from different technologies.

Tutorial sponsored by:



Rm: Fir Ballroom • 1:30 pm - 5:00 pm

Tutorial 5 • SystemC Transaction Level Modeling Standards and Methodology Guidelines

Organizer: John Aynsley - *Doulos Ltd.*

Presenters: John Aynsley - *Doulos Ltd.*
Stuart Swan - *Cadence Design Systems, Inc.*

Transaction Level Modeling (TLM) is important for architectural exploration and performance modeling, for building virtual prototypes of hardware platforms for early software development, and for writing testbenches for hardware verification. The first release "TLM1" of the OSCI TLM standard in 2005 provided a standard set of interfaces that permit plug-and-play between transaction-level components at the transport layer, particularly useful for untimed modeling in a verification environment.

The successful adoption of TLM depends on the interoperability of models from multiple sources at multiple abstraction levels. Right now, this means the ability to support models of common on-chip busses at the Programmers View (PV) level, to annotate timing onto those models (PVT), and to support Cycle Accurate (CA) modeling. Addressing the challenges of interoperability at these modeling levels has been the focus of the OSCI TLM Working Group over the past year, and this effort resulted in the first release of "TLM2" for public review in late 2006.

After a brief introduction to SystemC and TLM, this tutorial will present an in-depth discussion of the many technical issues raised and addressed by TLM2, will provide examples showing how TLM2 can be used to write interoperable models at the PV and PVT levels, and will offer guidelines for successful TLM modeling.

Agenda:

- A brief intro to SystemC and TLM plus the role of TLM today
- A review of OSCI TLM1 standard, and how to take advantage of TLM1 principles in practical modeling situations
- Discussion of the implementation of TLM2 using worked examples
- A glimpse at the new features of TLM2 for 2007
- A presentation from a TLM user on adopting TLM2

Wednesday Opening Reception



What a great opportunity to relax and visit with other influential people of the industry. Enjoy cocktails, meet new people, swap ideas, and learn something new.

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SYNOPSIS[®]

February 21, 5:00 pm - 7:00 pm
In the Vendor's Exhibit Area



Thursday, February 22, 2007

7:30 am - 8:45 am • DVCon Breakfast and Presentation sponsored by: **cadence** (Pine/Cedar Ballroom)

9:00

Keynote Address (Donner Ballroom)

Moshe Gavrielov - Executive VP and GM, Verification Division, Cadence Design Systems, Inc.

10:00

Break

Donner Ballroom

Oak/Fir Ballroom

10:30

Session 1

SystemVerilog for Design

Session 2

SystemC in Action

12:00

Lunch Panel • The Lowdown on Low-Power Design and Verification - Views from the Experts

sponsored by: **Mentor Graphics** (Pine/Cedar Ballroom)

1:30

Session 3

SystemVerilog Assertions

Session 4

Physical Layer Verification

3:00

Break

3:30

Panel 1 (Oak/Fir Ballroom)

The Bigwigs Panel

5:00

Exhibit hours: 4:00 pm - 7:00 pm (Cascade Ballroom)

Cocktail Reception in the Exhibit Area • 5:00 pm - 7:00 pm



Friday, February 23, 2007

Panel Session: Blended Coverage: A Recipe for Success (Donner Ballroom)			9:00
Break			10:00
Donner Ballroom	Cascade Ballroom	Siskiyou Ballroom	
Session 5 SystemVerilog DPI	Session 6 Formal Verification	Session 7 Advances in Research - I	10:30
			12:00
Lunch and Presentation sponsored by: cādence ™ (Oak Ballroom)			
Session 8 Advanced Stimulus Generation	Session 9 Real World Verification Applications	Session 10 Advances in Research - II	1:30
			3:00
Break			
Embedded Tutorial 1 Unifying Low-Power Design with UPF	Embedded Tutorial 2 Building a Transaction-Based Acceleration Regression Environment	Embedded Tutorial 3 Re-usable Performance Verification of Interconnect IP Design	3:30
			5:00
Closing Session (Donner Ballroom) 2007 Best Paper Award Presentation			

Opening Session/Keynote Address

Thursday, February 22, 2007

9:00 am

Rm: Donner Ballroom



Keynote Speaker

Taking An Enterprise-Wide Approach to Next-generation System-level Development

Moshe Gavrielov - Executive Vice President and General Manager, Verification Division,
Cadence Design Systems, Inc.

As we move from 65nm- to 45nm-based SoCs and beyond, we must dramatically expand the scope of the verification and next-generation digital design and implementation processes to avoid re-spins and expensive recalls. System-level complexities will increase the need for enterprise-wide verification solutions that link together and manage the hardware, software and system integration, and validation processes across many specialists. New interdependencies between verification, power management, test and physical design will increase the need for concurrent management of previously sequential processes isolated across many specialists. Moshe Gavrielov of Cadence Design Systems will discuss this new multi-specialist, enterprise-wide approach to automating and managing processes that promises to dramatically change the way that complex, advanced SoC IC designs are brought to market.

Moshe Gavrielov serves as Cadence Executive Vice President and General Manager, reporting to Michael J. Fister, President and CEO. He is responsible for the company's Verification Division.

Gavrielov has over 25 years of technology and business management experience, including serving as CEO of Verisity, Ltd. before joining Cadence in April 2005. Prior to joining Verisity, he worked nine years at LSI Logic, where he held several executive management positions. Those positions included executive vice president of the products organization, senior vice president of international markets, general manager of LSI Logic Europe and general manager of the ASIC division. Gavrielov received his Bachelor of Science degree in electrical engineering and a Masters degree in computer science from the Israel Institute of Technology (Technion) in Haifa, Israel.

Thursday, February 22, 2007

Session 1 ◦ SystemVerilog for Design

Rm: Donner Ballroom • 10:30 am - 12:00 pm

- 1.1** Designing a System-on-Chip with SystemVerilog in the Real World
Stefan Sandström - *Axis Communications AB*
- 1.2** Through the Looking Glass - A User's Perspective on System Verilog, SystemC
Bill Dittenhofer - *AMI Semiconductor*
- 1.3** Towards a Practical Design Methodology with SystemVerilog Interfaces and Modports
Jonathan Bromley - *Doulos Ltd.*

Session 2 ◦ SystemC in Action

Rm: Oak/Fir Ballroom • 10:30 am - 12:00 pm

- 2.1** Dramatically Increase the Performance of SystemC Simulations
Greg Tumbush, Mark Hupp - *AMI Semiconductor*
- 2.2** A Technique for Adding Functional Coverage to SystemC
Kurt Schwartz - *Willamette HDL, Inc.*
- 2.3** Space Codesign: A SystemC Framework for Fast Exploration of Hardware/Software Systems
Luc Filion, Marc-André Cantin, Laurent Moss, Guy Bois - *Ecole Polytechnique*
El Mostapha Aboulhamid - *Univ. of Montreal*



Design and Verification Conference and Exhibition

Thursday, February 22, 2007

DVCon Breakfast & Presentation

Rm: Pine/Cedar Ballroom • 7:30 am - 8:45 am

sponsored by:

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Lunch Panel

Rm: Pine/Cedar Ballroom • 12:00 pm - 1:30 pm

***The Lowdown on
Low-Power Design
and Verification -
Views from the Experts***

sponsored by:

**Mentor
Graphics®**

Thursday, February 22, 2007

Rm: Pine/Cedar Ballroom • 12:00 pm - 1:30 pm

Lunch Panel ○ The Lowdown on Low-Power Design and Verification - Views from the Experts

Moderator: Richard Goering - EDA Editor, EE Times

Organizers: Karen Bartleson - *Accellera Secretary, Si2*
Dennis Brophy - *Mentor Graphics Corp.*

lunch
sponsored by:



Arguably, power management is today's most critical area of integrated circuit design. Of all the issues facing chip and systems designers, none is more burning than the soaring levels of power flowing through their circuits. Many leading-edge designers believe that power has become the dominant factor in the design of modern electronic systems.

EDA vendors have offered various solutions to power management, each with different formats and methods for describing low power design intent. Likewise, leading chip companies are seeking new ways to manage low power in their newest chip designs, and demand a standard method to express low power design intent throughout the IC design flow.

Has there been actual progress on standards or has controversy clouded the vision of a fast, open standard? How do we ensure that low power verification technology uncovers design issues

before synthesis? And is this even possible when verification itself is still the critical bottleneck in the industry? Are customers satisfied with the solution so far? What more needs to be done?

The panelists are experts in the fields of low power design and electronic design standards. They are well-qualified to discuss the subject of low power design challenges. The Moderator, Richard Goering, has a keen interest in the topic and is an experienced panel moderator who poses intriguing and in-depth questions.

Panelists: John Goodenough - *ARM Ltd.*
Pankaj Mayor - *Cadence Design Systems, Inc.*
Thomas Blaesi - *ChipVision*
Gary Delp - *LSI Logic*
Harry Foster - *Mentor Graphics Corp.*
Mike Keating - *Synopsys, Inc.*

Session 3 ◦ SystemVerilog Assertions

Rm: Donner Ballroom • 1:30 pm - 3:00 pm

- 3.1 Using SystemVerilog Assertions for Creating Property-Based Checkers**
Dmitry Korchemny - *Intel Corp.*
Eduard Cerny, Angshuman Saha - *Synopsys, Inc.*
- 3.2 SVA Local Variable Coding Guidelines for Efficient Use**
Jiang Long, Andrew Seawright, Harry Foster - *Mentor Graphics Corp.*
- 3.3 Have I Placed All the Right Assertions in All the Right Places? Boosting Assertion Quality with Visual Flow Diagrams**
Roger Sabbagh - *Mentor Graphics Corp.*
Jim O'Connor - *iVivity, Inc.*

Session 4 ◦ Physical Layer Verification

Rm: Oak/Fir Ballroom • 1:30 pm - 3:00 pm

- 4.1 PHY Verification - What's Missing?**
Thomas Sheffler, Kathryn Mossawir, Kevin Jones - *Rambus Inc.*
- 4.2 Functionally PHYne? Verification Solutions for the Physical Layer**
Amit Chowdhry - *Advanced Micro Devices*
- 4.3 Sending Analog Values Along Digital Wires**
Chris Jones, Jeff McNeal, Ross Segelken - *Synopsys, Inc.*

Thursday, February 22, 2007

Rm: Oak/Fir Ballroom • 3:30 pm - 5:00 pm

Panel 1 ◦ The Bigwigs Panel

Moderator: John Cooley - ESNUG & EE Times, Holliston, MA

Officially the title to this panel is "The Bigwigs Panel". The reality is that it should be titled "The Cooley Panel - Where everyone Gets to see the EDA Bigwigs Run the Gauntlet of This Year's Difficult Questions" -- but that's too many words to put in a title.

Every year John Cooley gathers together bigwigs from most of the major and few minor companies. He then surveys his 25,000 member ESNUG mailing list for edgy questions to ask his panelists. Then Cooley asks the panelists the questions. It makes for one colorful afternoon of no BS discussions.

Panelists: To be announced.

Please join us at 5:00 pm after the panel for a reception in the exhibit hall, located in the Cascade Ballroom.

All are welcome!

Rm: Donner Ballroom • 9:00 am - 10:00 am

Panel 2 ◦ Blended Coverage: A Recipe for Success

Moderator: Harry Foster - *Mentor Graphics Corp.*

Verification, like an exotic blender concoction, is a multi-dimensional undertaking. The verification endeavor generally spans multiple levels of abstractions, evolves throughout a project's lifecycle, and depends on multiple tools and processes. In addition, success requires coverage metrics to determine the quality and completeness of the verification process, and serve two primary purposes:

1. Identify where we have been (that is, what functionality or implementation structures have been verified)
2. Identify how far we have to go (that is, where the verification process currently stands in terms of completion)

Yet measuring and analyzing coverage, like verification itself, is a multi-dimensional problem—whose recipe for success requires a skill in the art of managing and merging multiple views of data from multiple heterogeneous tools.

With the emergence of recent standards, such as the IEEE Std-1800 SystemVerilog, many verification teams are starting to integrate advanced coverage-driven verification techniques into their flows. Some teams focus entirely on manually specified functional coverage techniques—whose coverage space provides a mapping back to the project's architectural and micro-architectural specifications. Other teams focus on automatically extracted structural coverage techniques to ensure that the implementation is thoroughly exercised. Still other teams blend the multiple techniques in such a way to identify holes in their coverage model.

This panel offers a unique user's perspective of today's coverage problem. Our distinguished panel of industry sous chefs will examine the problems of coverage data management from various user project perspectives, and debate the best approaches for blending coverage.

Panelists: David Lacey - *Hewlett-Packard Co.*
Jerry Vauk - *Advanced Micro Devices*
Prakash Rashinkar - *Rambus Inc.*
Vigyan Singhal - *Oski Technology*
Peter Lafauci - *Mentor Graphics Corp.*

Friday, February 23, 2007

Session 5 ◦ SystemVerilog DPI

Rm: Donner Ballroom • 10:30 am - 12:00 pm

- 5.1** Inter-Language Function Calls between SystemC and SystemVerilog
Rich Edelman, Mark Glasser, Arnab Saha, Hui Yin - *Mentor Graphics Corp.*
- 5.2** A Reusable Real-Time GUI Scoreboard for Your Self-Checking Testbench Using the SystemVerilog DPI
Tom Austin - *Plexus*
- 5.3** Hardware/Firmware Co-Verification Using ISS Integration and a SystemVerilog DPI
Arthur Freitas - *Hyperstone AG*

Session 6 ◦ Formal Verification

Rm: Cascade Ballroom • 10:30 am - 12:00 pm

- 6.1** Benevolently Equivalent: Effectively Using Logic Equivalence in Your Design Flow
Amit Chowdhry - *Advanced Micro Devices*
- 6.2** FEV's Greatest Bloopers: False Positives in Formal Equivalence
Erik Seligman, Joonyoung Kim - *Intel Corp.*
- 6.3** Complete Formal Verification of TriCore2 and Other Processors
Adriana Maggiore - *OneSpin Solutions GmbH*

Session 7 ◦ Advances in Research - I

Rm: Siskiyou Ballroom • 10:30 am - 12:00 pm

- 7.1 System-level Synthesis from Transaction-level Models: Algorithms and Tools**
Rainer Doemer, Daniel D. Gajski -
Univ. of California, Irvine
- 7.2 On the Automatic Transactor Generation for the TLM-based Design Flow**
Franco Fummi, Nicola Bombieri -
Universita di Verona
- 7.3 A Prototypic Language for Transaction Level Assertions**
Wolfgang Ecker, Volkan Esen, Michael Hull,
Thomas Steininger, Michael Velten -
Infineon Technologies AG

Corporate Sponsors



**Attendee Bag,
Thursday Breakfast,
Friday Lunch**

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Friday, February 23, 2007

Session 8 ◦ **Advanced Stimulus Generation**

Rm: Donner Ballroom • 1:30 pm - 3:00 pm

- 8.1 Advanced Stimulus Generation Using Scenarios**
Pierre Girodias, Hans van der Schoot, Amre Sultan - *XtremeEDA Corp.*
- 8.2 An Architecture for Complex Multi-Channel Stimulus Generation**
Mark Glasser - *Mentor Graphics Corp.*
- 8.3 A Flexible and Interoperable Testbench Phasing Methodology using the AVM**
Peter Lafauci, Adam Rose - *Mentor Graphics Corp.*

Session 9 ◦ **Verification Applications**

Rm: Cascade Ballroom • 1:30 pm - 3:00 pm

- 9.1 Adelante VD3204x Core, SubSystem and SoC Verification: What is Verified Where, Why and How?**
Roger Witlox, Ronald Heijmans, Chris Wieckardt - *NXP Semiconductors*
- 9.2 Verification of a next-generation single-chip Analog TV and Digital TV ASIC**
Yj Patil - *Genesis Microchip Inc.*
Dean D'Mello - *Cadence Design Systems, Inc.*
- 9.3 Challenges and Practical Lessons Learned in the Verification and Validation of an Ultra-High Performance Physics Processing ASIC**
Badri Gopalan, Otto Schmid, Monier Maher, Yu Shan, William Bean, Sanjay Patel - *Ageia Technologies*
Mahesha Puttanna - *Wipro Technologies*

Session 10 ◦ Advances in Research - II

Rm: Siskiyou Ballroom • 1:30 pm - 3:00 pm

- 10.1 Assessment of Real-Time Operating Systems Characteristics in Embedded Systems Design by SystemC models of RTOS Services**
Sorin A. Huss - *Technical Univ. of Darmstadt*
Stephan Klaus - *ISRA Vision Ltd.*
- 10.2 Low Maintenance Verification**
Valeria Bertacco - *Univ. of Michigan*
- 10.3 A Next-Generation Design Framework for Platform-Based Design**
Abhijit Davare, Douglas Densmore, Trevor Meyerowitz, Alessandro Pinto, Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley*

Embedded Tutorial 1 ◦ Unifying Low Power Design with UPF

Rm: Donner Ballroom • 3:30 pm - 5:00 pm

Stephen Bailey - *Mentor Graphics Corp.*
Jim Sproch - *Synopsys, Inc.*

Power is the number one design driver. Multiple solutions have evolved for capturing low power design intent, verification and implementation. The incompatible solutions create redundant work and potential for bugs through inconsistency and obsolescence. This tutorial covers the Unified Power Format (UPF), an open standard developed by Accellera, and how it can be used throughout a low power design flow.

Friday, February 23, 2007

Embedded Tutorial 2 ◦ Building Transaction-Based Acceleration Regression Environment using Plan-Driven Verification Approach

Rm: Cascade Ballroom • 3:30 pm - 5:00 pm

**Shabtay Matalon, Maya Bar, Kanwarpreet Grewal,
Leonard Drucker** - *Cadence Design Systems, Inc.*

The tutorial presents flows and methodologies for using plan-driven verification testbenches with accelerated verification engines via transaction oriented interfaces. It describes how to reuse stimuli generation, coverage analysis, checking and error handling in reactive and regression environments while optimizing the testbench architecture and modeling style for high performance verification.

Embedded Tutorial 3 ◦ Re-usable Performance Verification of Interconnect IP Designs

Rm: Siskiyou Ballroom • 3:30 pm - 5:00 pm

**Sriram Swaminathan, Yogendhar K.,
Vidhya Thyagarajan** - *Rambus Chip Technologies
India (Pvt.) Ltd.*

This tutorial discusses the importance of performance verification in the early stages of the design cycle to avoid re-spins due to performance issues. The paper focuses on reusable third-party design IPs and describes the challenges involved in verifying a configurable interconnect IP for performance and presents a case study of performance analysis setup for a PCI Express IP based system. The case study presents a configurable and re-usable performance verification setup and how various performance metrics such as roundtrip latency and bandwidth can be used to characterize an IP.

Exhibits

Exhibiting Companies

Aldec, Inc.	# 301
ArchPro Design Automation, Inc.	# 402
Averant, Inc.	# 304
Axiom Design Automation	# 803
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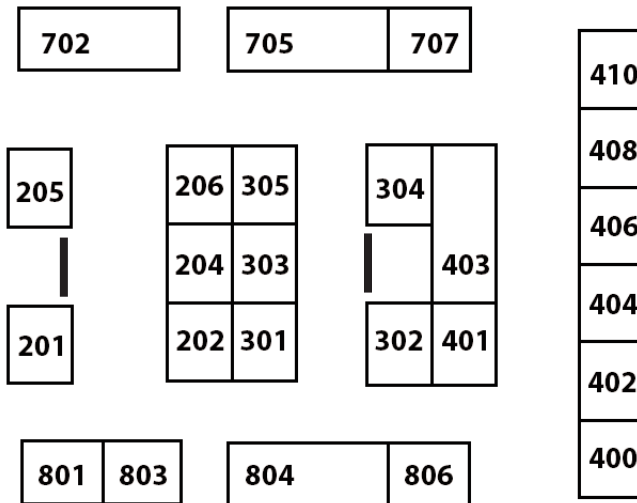
Exhibit Hours (Cascade Ballroom)

Wednesday, February 21, 2007 4:00 pm - 7:00 pm

Thursday, February 22, 2007 4:00 pm - 7:00 pm

The DVCon 2007 Exhibition consists of vendors displaying the latest in Hardware Description Languages, Hardware Verification Languages and EDA tools for the design and verification of electronic systems and integrated circuits.

Exhibit Floorplan



Exhibits

Aldec, Inc.

Booth # 301

2260 Corporate Cir.

Henderson, NV 89074

702-990-4400

www.aldec.com

Since 1997, Aldec has been focused on providing easy-to-use VHDL and Verilog design entry and simulation products to support programmable logic designers. Aldec provides a broad spectrum of HDL verification tools to support every market segment, ranging from entry-level HDL users who target low density FPGAs to users requiring high performance tools for Assertion-based verification designs, as well as hardware-based acceleration and co-verification methodologies to best meet their time to market requirements.

ArchPro Design Automation, Inc.

Booth # 402

1425 McCandless Dr.

Milpitas, CA 95035

408-717-4911

www.archpro-da.com

ArchPro has developed a comprehensive low power management verification tool suite, built upon MVSIM™, MVRC™ and MVSYN™— tools that are uncovering fatal design issues, not found by other industry tools, in the architectural/RTL/gate level of the design cycle – saving months in product development cycles by eliminating chip respins and expensive silicon debug time. ArchPro's products are silicon proven on the most advanced power management techniques available today: voltage islands, power gating, dynamic and adaptive voltage frequency scaling, body bias, low Vdd standby, etc.



Design and Verification Conference and Exhibition

Exhibits

Averant, Inc.

Booth # 304

22320 Foothill Blvd.

Hayward, CA 94541

510-581-8881

www.averant.com

Averant provides the most technologically advanced Static Functional verification tool available today. Averant's flagship product, Solidify™, delivers unprecedented performance in the functional verification of Verilog and VHDL designs. Solidify supports the PSL, SVA, and OVL assertion languages, includes a series of easy-to-use automatic checks, and offers the industry's only patented coverage option for formal verification. Averant also markets SolidPC™, a static protocol checker for the AMBA bus protocol. Jointly developed with ARM, SolidPC has earned "AMBA 3 Assured™" logo certification.

Axiom Design Automation

Booth # 803

1900 McCarthy Blvd., Ste. 207

Milpitas, CA 95035

408-433-9997

www.axiom-da.com

AXIOM is a pioneer in developing functional verification products offering an integrated verification environment that combines the fastest simulator in the industry with advanced testbench automation, assertion based verification, debugging and coverage analysis to ensure that your most complex designs are fully verified in the least amount of time.

AXIOM supports commercially available hardware and industry standard languages including SystemVerilog, Verilog and OpenVera to ensure continuity with your existing verification methodology while offering a clear path to immediate productivity improvement.



Cadence Design Systems, Inc.

Booth # 403

2655 Seely Ave.

San Jose, CA 95134

408-943-1234

www.cadence.com

Cadence Design Systems is the world's leading EDA technologies and engineering services company. Cadence helps its customers break through their challenges by providing leading edge electronic design solutions that speed advanced IC and system designs to volume production. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, printed circuit boards and systems used in consumer electronics, networking and telecommunications equipment, and computer systems.

Consultants' Corner

Booth # 705

Sutherland HDL, Inc.

22805 SW 92nd Pl.

Tualatin, OR 97062

503-692-0898

www.sutherland-hdl.com

Sutherland HDL provides SystemVerilog training and consulting. Our training workshops are developed and presented by experts with substantial experience in design and verification. The lab-intensive workshops emphasize writing correct code and avoiding gotchas. Workshops include "Verilog with SystemVerilog for Synthesis", "SystemVerilog for Design Engineers", "SystemVerilog Testbench for Verification Engineers", and "SystemVerilog Assertions for Design and Verification". Workshops can be presented at your company, anywhere in the world. Check our web site for open-enrollment workshop schedules. Contact Stuart Sutherland, stuart@sutherland-hdl.com, 1-866-HDL-XPRTS.

Consultants' Corner

Booth # 705

XtremeEDA Corp.

555 Legget Dr., Tower B, Ste. 140,

Kanata, ON, Canada, K2K 2X3

613-254-9685

www.xtreme-eda.com

XtremeEDA Corporation is a professional services firm that provides world-class functional verification expertise. Our industry-leading consultants have decades of experience in verification planning, architecture and testbench implementation. Experts in all HVLs and advanced methodologies, we provide migration and training services. We help clients migrate from any HDL or HVL to SystemVerilog with our XtremeBoost service and our flagship SystemVerilog for Verification Professionals course. Visit us at the consultants corner, at www.xtreme-eda.com or call Claude Cloutier at 604-773-1522 to learn more.

Doulos

Booth # 204

16165 Monterey Rd.

Morgan Hill, CA 95037

888-GO-DOULOS

www.doulos.com

Doulos is the global leader for the development and delivery of world class training solutions for SoC, FPGA and ASIC design and verification. Fully independent, Doulos sets the industry standard for high quality training in SystemCTM, SystemVerilog, e, PSL, Verilog®, VHDL, Perl & Tcl/Tk.

Since 1991, Doulos has contributed to the success of more than 600 companies across 30 countries. The natural partner for leading tool and technology companies, Doulos schedules classes across the U.S and delivers in-house training world-wide.

Exhibits

EVE

Booth # 404

84 W. Santa Clara St., Ste. 580

San Jose, CA 95113

408-881-0440

www.eve-usa.com

Verification hot box – up to 200 screaming MHz. EVE offers the fastest verification and most cycles per dollar. Run your full chip testbenches at MHz speed, verifying hardware and software together, before tapeout. EVE's ZeBu™ (Zero Bugs) platform handles hardware debug, regression testing, HW/SW integration, and SW development. Cover both emulation and ASIC prototyping needs with a single, affordable platform. Learn why so many ESNUG users are raving and why 8 out of the top 10 semiconductor companies use EVE.

GiDEL Inc.

Booth # 801

1600 Wyatt Dr., Ste. 1

Santa Clara, CA 95054

408-969-0389

www.gidel.com

GiDEL provides Powerful Development Tools and Universal FPGA Platforms for Custom/ASIC Rapid Prototyping, Verification, Emulation, Co-Design, Simulation Acceleration, Vision/DSP Systems and Algorithm Development. GiDEL also provides High Productivity Software Tools and IPs that compliment High-Performance PCI and Stand-Alone boards, offering outstanding Cost/Performance Advantages and time to market solutions. These Innovative Development Methodologies and our expertise at System Level Integration is valuable to companies needing to verify ASIC Designs or Building System-Level Boards.

HARDI Electronics

Booth # 302

26831 Magdalena Ln.

Mission Viejo, CA 92691

949-202-5572

www.hardi.com

HARDI ASIC Prototyping System (HAPS) provides best-in-class flexibility and connectivity for ASIC prototyping and emulation. HAPS is the first modular FPGA board system providing high speed, high capacity, and real-time debugging. The system is composed of FPGA motherboards with massive connectivity and a large selection of off-the-shelf daughter boards, giving designers virtually the same functionality as the ASIC. To accommodate very large designs, designers can connect a number of motherboards in many different ways. For more information about HAPS, please visit: <http://www.hardi.com>.

Jasper Design Automation, Inc.

Booth # 201

100 View St., Ste. 101

Mountain View, CA 94041

650-966-0200

www.jasper-da.com

Jasper Design Automation's JasperGold® Verification System is the first verification product to deliver complete "deep formal" systematic verification, ensuring design correctness where it matters most. Requiring no testbench development, JasperGold formally verifies that complex IC design blocks meet high-level requirements defined in their specifications, and also pre-verifies IP blocks for all usage modes. Jasper's formal ABV solution, JasperGold® Express, provides the industry's leading "light formal" solution, complementing simulation to accelerate bug-hunting and coverage attainment. For more information, visit <http://www.jasper-da.com>.

Exhibits

JEDA Technologies

Booth # 205

4962 El Camino Real, Ste. 105

Los Altos CA 94022

650-964-5332

www.jedatechnologies.net

JEDA is focused on SystemC verification automation. NSCv provides in-line dynamic treading with memory management and data coverage to SystemC. NSCv fixes the fundamental threading limitations and memory management problems in SystemC and addresses some of missing capabilities in the commercially unsupported SCV (SystemC Verification Library).

NSCa is a comprehensive native SystemC assertion development and debug environment for transaction-level and cycle-level design. NSCa enables the architect/systems engineer to create system-level checks that are used throughout the design and verification cycles.

Mentor Graphics Corp.

Booth # 804

8005 SW Boeckman Rd.

Wilsonville, OR 97070

503-685-1907

www.mentor.com

Mentor Graphics® is the industry's functional verification leader, providing best-in-class technologies and methodologies based on industry standards such as SystemVerilog and SystemC. The Mentor Graphics Questa™ advanced verification environment, combined with Mentor's 0-In® functional coverage tools, deliver the most comprehensive verification flow in the industry. The Mentor Graphics Advanced Verification Methodology (AVM) is the first, true, system-level-to-RTL verification methodology that enables leading-edge verification technologies to designs at multiple levels of abstraction, using multiple languages. The AVM provides libraries of base classes and modules in open-source and uses TLM interfaces as the communication mechanism between verification components. Mentor's portfolio of electronic system level (ESL) design technologies complement the AVM to enable hardware design and verification at a higher lever of abstraction. For more information, go to www.mentor.com.

Nascentric

Booth # 406

15911 Ruel Cove

Austin, TX 78759

512-225-8775

www.nascentric.com

Nascentric invites you to see AuSIM™, a 4th generation Fast-SPIICE simulator. AuSIM's patent-pending technology, multi-engine architecture, multi-threaded algorithms, and advanced parasitic handling maximize runtime performance, increase accuracy, and improve simulation capacity. Up to 10X faster than traditional Fast-SPIICE simulators AuSIM exceeds the accuracy and capacity requirements needed for leading-edge designs; thus helping to eliminate costly silicon re-spins. For more information on AuSIM, please visit us in Booth 406 OR visit our website at: www.Nascentric.com

Novas Software, Inc.

Booth # 202

2025 Gateway Pl., Ste. 400

San Jose, CA 95110

408-467-7888

www.novas.com

Novas Software, Inc. is the leading provider of design comprehension solutions for engineers designing complex ICs, embedded systems and SoCs. Novas' Verdi automated debug and Siloti visibility enhancement products dramatically accelerate the process for understanding and correcting design problems starting from system-level specification through silicon implementation.



OneSpin Solutions GmbH

Booth # 401

Theresienhoehe 12

Munich 80339 Germany

+49-89-99013-0

www.onespin-solutions.com

OneSpin Solutions demonstrates its field-proven OneSpin 360™ Module Verifier formal verification solution - the first to systematically detect all functional errors in complex digital modules and intellectual property. The demonstration shows how 360 MV efficiently detects all gaps in complex verification plans using automatic completeness analysis. OneSpin will also present a new highly automated equivalence checking product - extending its well-established, synthesis independent 360 Equivalence Checker - that preserves design quality through subsequent implementation and optimization phases.

ProDesign Electronics Corp.

Booth # 305

2107 N. First St., Ste. 380

San Jose, CA 95131

408-441-7880

www.prodesign-usa.com

The privately held company was founded in 1981 and has over 90 employees, with facilities for research, design, and sales in Germany, France and the U.S. ProDesign has more than twenty-four years of experience as a service provider and manufacturer in the electronics industry. The company's products and services include the CHIPit family of hardware-assisted verification tools to validate algorithm performance, verify hardware implementation, and assist in hardware/software co-development to reduce the verification time dramatically.

Real Intent, Inc.

Booth # 806

505 N. Mathilda Ave., Ste. 210

Sunnyvale, CA 94085

408-830-0700

www.realintent.com

Real Intent is the leading provider of static and assertion-based formal verification solutions. Real Intent's products dramatically improve the functional verification efficiency of ASIC, SOC, and FPGA devices.

EnVision: Ascent & Conquest are static formal Assertion Based Verification (ABV)

EnVision: Clock Intent Verification is clock domain crossing verification

EnVision: PureTime is verification of Timing Exception Constraints.

Over 40 major electronic design houses, including Sun Microsystems, AMD, Marvell Technology, nVidia, and NEC Electronics rely on Real Intent solutions.

Springer Science & Business Media, LLC

Booth: Lobby

101 Philip Dr., Assinippi Park

Norwell, MA 02061

866-269-9527

www.springer.com

11 New verification books from Springer for DVCon 2007 include:

Writing Testbenches Using SystemVerilog, Bergeron
A Roadmap for Formal Property Verification, Dasgupta
A Practical Introduction to PSL, Eisner/Fisman
Computation Engineering: Applied Automata Theory and Logic, Gopalakrishnan
Hardware Verification with C++, Mintz/Ekendahl
SystemVerilog for Verification, Spear
SystemVerilog for Design, Second Edition, Sutherland/Davidmann/Flake
Effective Functional Verification, Vasudevon
Constraint-Based Verification, Yuan/Pixley/Aziz
Creating Assertion Based IP, Foster/Krolnik
Metric Driven Design Verification: An Engineer's and Executive's Guide to First Pass Success, Carter/Hemmady



Synopsys, Inc.

Booth # 702

700 E. Middlefield Rd.

Mountain View, CA 94043

650-584-5000

www.synopsys.com

Delivering a New Level of Verification Excellence for Complex Chip Design

The Discovery™ Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, DesignWare® VIP, code coverage, functional coverage, testbenches and formal analysis. Combined with support for industry standard languages, including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®, and the VMM Methodology, the Discovery Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

Synplicity, Inc.

Booth # 303

600 W. California Ave.

Sunnyvale, CA 94086

408-215-6000

www.synplicity.com

Synplicity is a leading supplier of innovative software solutions that enable the rapid and effective design and verification of Programmable Logic devices including those used for FPGA-based ASIC verification. Synplicity's products are used in communications, military/aerospace, consumer, semiconductor, computer and other electronic systems markets. Synplicity's tools provide outstanding performance, cost and time-to-market benefits by simplifying, improving and automating key design planning, logic synthesis, physical synthesis and verification functions for FPGA, FPGA-based ASIC verification, and DSP designers.

The Dini Group

Booth # 707

1010 Pearl St., Ste. 6

La Jolla, CA 92037

858-454-3419

www.dinigroup.com

The Dini Group products feature the most advanced Xilinx and Altera FPGA's configured in the most usable way. Our experience with application partitioning and real time data management is reflected in the high speed interconnects and useful architecture of our hardware. Most of our products break the 1-cent/ASIC gate barrier.

Veritools, Inc.

Booth # 206

459 Hamilton Ave., Ste. 200

Palo Alto, CA 94301

650-462-5590

www.veritools.com

Improve your rate of first silicon success with Veritools new product, VeritoolsVerifyer. This software supports coverage driven verification with SystemVerilog Assertion evaluation, analysis, coverage and correlation tools. Additionally, our RTL source code debugging environment for Verilog, VHDL and SystemVerilog, VeritoolsDesigner, increases productivity with Waveform windows, Schematic windows, State Diagrams, Source Code Browser, Perl Scripting, and more. Veritools data formats provide instantaneous load and display as well as file compression up to 1,300x. Most digital and analog simulators are supported on a wide variety of platforms.

February 21 - 23, 2007 • DoubleTree Hotel, San Jose, CA
Additional Meetings/Conference Management



XenoTech Software

Booth # 408

441 28th St.

San Francisco, CA 94131

415-867-9506

www.xlxsolutions.com

XenoTech Software brings to the North American market SoC (System-on-Chip) design and system integration verification products. Initially developed and deployed in Europe, these Verification Intellectual Property (VIP) products and Verification Kits have proven to improve the productivity of SoC verification teams, reduce the cost of SoC development and significantly improve the quality of designs before going to tape-out.

XenoTech Software is proud to have been selected as the representative for Globetech Solutions, HDL Design House, and Yogitech - VIP industry leaders.



Design and Verification Conference and Exhibition

Additional Meetings/Conference Management

ADDITIONAL MEETINGS

North American SystemC Users Group

NASCUG VI Meeting

Wednesday, February 21 8:00 am - 1:00 pm Fir Ballroom

NASCUG provides a forum for users to contribute and interact. User presentations discuss design, modeling and verification with SystemC. NASCUG will be held February 21 and is free.

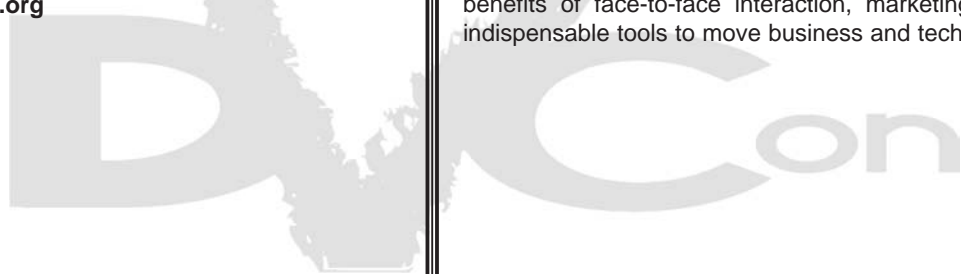
To register: www.nascug.org

CONFERENCE MANAGEMENT

MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
303-530-4562
www.mpassociates.com

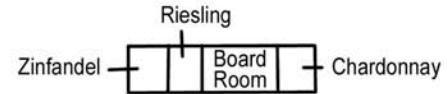
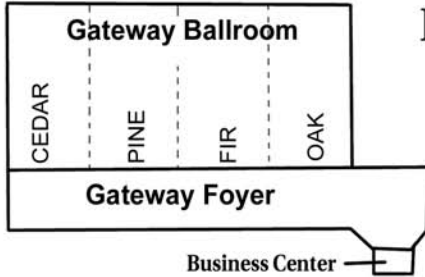


MP Associates, Inc. (MPA) brings people together through conferences and trade shows to solve problems, advance the state-of-the-art, make deals, and build industries. We believe in the benefits of face-to-face interaction, marketing, and education as indispensable tools to move business and technology forward.

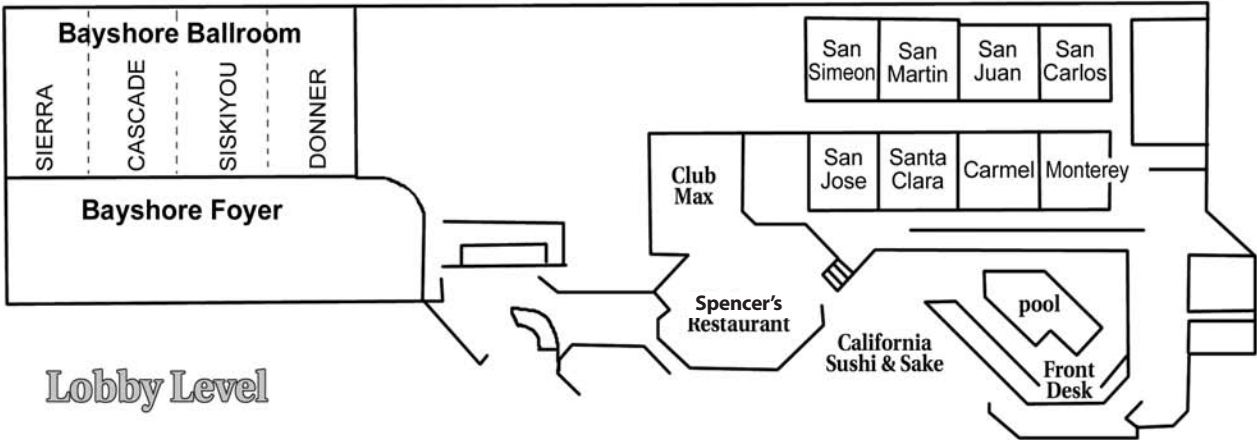


Hotel Floorplan

DoubleTree Hotel, San Jose, CA



Second Level



Lobby Level

Synopsys