



2008 Design and Verification Conference Attendee Questionnaire Results

1) Which is your primary design language?

Verilog	55%
VHDL	10%
C/C++	12%
SystemC	8%
SystemVerilog	15%

4) Which primary property specification (assertion-based verification) language do you use?

Verilog	34%
VHDL	6%
PSL	10%
SystemVerilog (SVA)	50%
Other	

2) Which primary verification language do you use?

C/C++	18%
E	5%
OpenVera	4%
Verilog	25%
VHDL	7%
System C	11%
SystemVerilog	30%
Other	

5) What design area(s) are you focused on? (Check all that apply)

Systems Design	12%
Standard ICs	5%
ASICs	19%
DSP Design	3%
Microprocessor/Microcontroller Design	6%
FPGAs & PLDs	9%
Multi-Chip Modules	2%
PCBs	2%
Library Development	2%
Analog/Mixed Signal	4%
EDA Tools	10%
Verification	16%
SOCs	10%
Other	

3) Which primary verification language do you plan to use for your next design?

C/C++	15%
e	4%
OpenVera	2%
Verilog	16%
VHDL	5%
SystemC	11%
SystemVerilog	47%
Other	

6) What on-chip buses do you intend to use in the next 12 months?

AMBA 2.0 AHB/APB	20%
AMBA 3 AXI	14%
OCP 2.0	5%
OCP 2.1	6%
CoreConnect	3%
Others/Proprietary	21%
None	31%

7) What interfaces standards do you expect to use in the next 12 months?

PCI Express 1.1	8%
PCI Express 2.0	16%
USB 2.0/OTG	13%
Serial ATA	7%
10G Ethernet	8%
10/100/1G Ethernet	12%
Wireless USB	5%
PCI/PCI-X	7%
CE-ATA	1%
None	23%

8) What is the size in gates of your current/last design?

Not applicable	36%
<1M	10%
1 – 3M	9%
3 – 5M	8%
5 – 10M	12%
10 – 50M	15%
>50M	10%

9) How many clock domains do your designs average?

1	20%
2	9%
2-5	32%
5-10	22%
10-20	7%
>20	10%

10) What is your number one design constraint?

Low power	34%
Size/density	20%
Performance /throughput	46%
Other	0%

11) What are the two main reasons for your attendance at DVCon? (Check all that apply)

Learn new techniques to improve your design process	33%
Learn new methodologies to improve your verification process	21%
Learn about new developments in design tools	17%
Meet and network with other engineers in the Industry	18%
Learn about industry in general	11%

12) Which category most closely describes your job description?

Senior management	16%
Engineering management	19%
Design engineer	17%
System architecture	3%
Marketing & sales	13%
Research/academic	4%
CAD	7%
Verification engineer	21%