



2009 Design and Verification Conference Attendee Questionnaire Results

	Percents
Which is your primary design language? (Pick one)	
Verilog	53%
VHDL	9%
C/C++	13%
SystemC	6%
SystemVerilog	19%
Which primary verification language do you currently use? (pick one)	
C/C++	16%
e	4%
OpenVera	4%
Verilog	25%
VHDL	6%
SystemC	9%
System Verilog	37%
Which primary verification language do you plan to use for your next design? (Pick one)	
C/C++	14%
e	4%
OpenVera	2%
Verilog	18%
VHDL	5%
SystemC	10%
SystemVerilog	48%
Which primary property specification (assertion-based verification) language do you use or plan to use?	
Verilog	31%
VHDL	8%
PSL	8%
SystemVerilog (SVA)	54%
What design area(s) are you focused on? (Check all that apply)	
Systems Design	11%
Standard ICs	4%
ASICs	17%
DSP Design	4%
Microprocessor/Microcontroller Design	7%
FPGAs & PLDs	11%
Multi-Chip Modules	2%
PCBs	3%
Library Development	2%
Analog/Mixed Signal	3%
EDA Tools	13%
Verification	14%
SOCs	9%
What on-chip buses do you intend to use in the next 12 months?	
AMBA 2.0 AHB/APB	19%
AMBA 3 AXI	15%
OCP 2.0	5%
OCP 2.1	7%
CoreConnect	4%
Others/Proprietary	18%
None	32%

	Percents
What standard interface do you expect to use in the next 12 months?	
PCI Express 1.1	7%
PCI Express 2.0	18%
USB 2.0/OTG	11%
Serial ATA	8%
10G Ethernet	9%
10/100/1G Ethernet	11%
Wireless USB	5%
PCI/PCI-X	6%
CE-ATA	1%
None	24%
What is the size in gates of your current/last design? (Pick one)	
Not Applicable	36%
<1M	10%
1 - 3M	8%
3 - 5M	8%
5 - 10M	13%
10M - 50M	15%
>50M	8%
How many clock domains do your designs average?	
1	14%
2	11%
2 - 5	35%
5 - 10	22%
10 - 20	9%
>20	9%
What is your number one design constraint?	
Low power	39%
Size/density	15%
Performance/throughput	46%
What are the two main reasons for your attendance at DVCon?	
Learn new techniques to improve your design process	16%
Learn new methodologies to improve your verification process	23%
Learn about new developments in design tools	20%
Meet and network with other engineers in the industry	23%
Learn about industry in general	17%
Which category most closely describes your job description? (Pick one)	
Senior Management	18%
Engineering Management	16%
Design Engineer	18%
System Architecture	5%
Marketing & Sales	17%
Research/Academic	3%
CAD	6%
Verification Engineer	17%