2017 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2017
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	23%
Standard IC Design	9%
ASIC /SoC Design	36%
DSP Design	5%
Microprocessor/Microcontroller Design	11%
IP Development	18%
Library Development	6%
Analog/Mixed Signal	11%
EDA Methods & Tools	29%
Verification	60%
FPGAs & PLDs	21%
Multi-Chip Modules	4%
PCB Design	6%
Software/Embedded Software	13%
Student	4%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	14%
Engineering Management	16%
Design Engineer	11%
System Architecture	3%
Application Engineer	4%
Marketing	4%
Technical Marketing	2%
Product Marketing	3%
Sales	5%
Research/Academic	2%
CAD	3%
Verification Engineer	28%
Software Engineer	3%
Student	3%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	40%
<1M	9%
1 - 5M	7%
5 - 10M	6%
10M - 50M	10%
50 - 100M	8%
>100M	20%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	51%
VHDL	17%
C/C++	34%
SystemC	16%
SystemVerilog	67%
e	5%
Not Applicable	16%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	56%
OVM	2%
VMM	2%
SystemC/TLM	5%
Proprietary	11%
Not Involved	24%

FIRST-TIME ATTENDEE

Yes	34%
No	66%