Verification Continuum Platform

Visit Synopsys at Booth #101
Welcome to DVCon

Dennis Brophy
General Chair - Mentor, a Siemens Business

Bigger and Better!

*Bigger and Better* applies to DVCon U.S. 2018, but the fact is the electronic systems you design and verify grow bigger and better every year as well. It is no accident that DVCon U.S. has grown, too to keep pace with you! I am happy to share many of the details of additions we have made to DVCon U.S. to add topics of importance that are motivated by the designs you are working on today and the systems you are creating for tomorrow. We have been with you at the start of the smartphone, PC and tablet era and are with you now as new huge market potentials are on the horizon for the Internet of Things (IoT), wearable systems and intelligent embedded systems that are on a path to support fully autonomous vehicles.

From Humble Beginnings

We have seen a lot together as DVCon U.S. celebrates its 30th birthday milestone this year! The first VHDL Users Group meeting was held at the 1988 Design Automation Conference in Anaheim, CA USA during a birds-of-a-feather session. From there it has grown to be known as DVCon now being held in the United States, Europe, India and China. After that 1988 meeting, VHDL was joined by Verilog with promotion arms created for both languages. A language war was presided over and peace in a bilingual/multilingual world was embraced. From a small start, a panoply of DVCons now reach thousands of practicing design and verification engineers around the world annually. It is humbling to be part of this growth and success and even more humbling to help all design and verification engineers be that much more productive and successful.

Having been in the industry in 1988, I do recall the planning that went into the 1988 meeting, but, personally, I have no memory of attending it. If you were there in the beginning or perhaps “not yet born” or “barely out of diapers” as would be the case with younger attendees, I can assure you that this event continues to bring users together to raise awareness of design and verification challenges and share solutions from fellow engineers and tool suppliers. It is this exchange of information that brings attendees back year after year. DVCon U.S. 2018 is a highly informative and educational event we hope you will attend.

Conference Highlights

As General Chair, I am privileged to represent the work of the Steering Committee and Technical Program Committee members. They do most of the work to form the conference content with help from our conference management company, MP Associates. The following are highlights for this year.

Keynote: Christopher Tice, vice president of Verification Continuum Solutions in the Verification Group at Synopsys will deliver this year’s keynote, “Industry's Next Challenge: The Petacycle Challenge.” This is the first time Mr. Tice will address DVCon. Mr. Tice is a longstanding and respected industry executive who has a focus to drive solutions in fast-growing verticals such as automotive, networking and IoT. Mr. Tice greatly complements this year’s program content and the future we look forward to creating.

Tutorials & Short Workshops: Of the four days of DVCon, the first and last day offer tutorials. New for this year are Short Workshops on the fourth day. The first day of tutorials is colloquially referred to as Accellera Day. This year Accellera sponsors a morning and afternoon tutorial. The morning tutorial will cover its emerging Portable Test and Stimulus standard and the afternoon will focus on the popular Universal Verification Methodology (UVM) and the work Accellera has done to complete its IEEE-1800.2™-2017 (the IEEE name for UVM) compatible reference implementation. On the fourth day of the conference, there will be six tutorials with a large focus in the afternoon on design and verification targeted at autonomous automobiles and the impact of functional safety requirements on those systems. Are there any bets on when and who will be the first person to come to DVCon in a fully autonomous vehicle?

We added the Short Workshop concept to draw more topics to provide attendees more opportunities to join in discussions and learning exercises that would not be as long and comprehensive as full tutorials. The four Short
Workshops on Thursday include topics on Deep Learning for the Design & Verification Engineer, Formal Verification, Mutation Coverage for Advanced Bug Hunting and one that will seek to have the design and verification engineer focus on getting the job done without concern that underlying it all is formal technology.

Technical Papers and Posters: From novice to expert, you are covered. Design and verification practitioners are set to cover popular topics in the formal paper presentation sessions and the ever popular poster sessions. The topics covered include UVM, functional and formal verification, high-level synthesis, C/C++/SystemC, assertion based verification, Portable Stimulus, safety critical verification and ISO 26262 fault analysis, advances in low-power design and verification. The RISC-V processor core even makes an appearance with a paper on its UVM-based verification model. You will certainly find something in the program that will help in your daily design and verification activities. You get to vote on best paper and poster awards to recognize the best-of DVCon. Authors are greatly appreciative of the recognition. This year we have shared some best practices for presenters on how they can deliver better presentations. We hope this shows. If this works, we may have made your job to discern the best paper and best poster just that much more difficult.

Panel Discussions: We have two panels this year, and both will be on the third day of the conference. The first panel reflects the issue that has come with the advent of large designs: Big Data. The more and more verification information that is generated, the harder it is to find root causes to problems or system flaws. With so much information being generated, you may find it hard to attain the system coverage you seek. The panel will be a good way for industry experts to explore this more. The second panel will explore the right tool for the hardest verification jobs. This reminds me of the old adage that says “if all you have is a hammer, everything looks like a nail.” The good news for design and verification engineers is that there are many tools to choose from and the panel should help us understand which tool is best for which task. And for both panels, we will be ready and open for questions from the floor. This is your time to speak too!

Exhibits: We have just about every inch of exhibit space covered. This makes for exciting social interactions after the conference program ends, during the evening receptions or during breaks. It is a good venue for business meet-ups when the conference is in session. You will find the latest in EDA tools, design and verification IP and services represented. Armed with what you have learned in the conference setting, the exhibitors will be ready to share their advances that might help you with many of your pressing design and verification issues. Whether you are in the exhibit area or connecting with peers at the hosted lunches, you will have many opportunities to network with your peers and learn from each other.

Thank You
On behalf of the DVCon U.S. 2018 Steering Committee and Technical Program Committee, I want to thank the hundreds, if not thousands of those who worked on or supported prior conferences from 1988 until today. It is their hard work and dedication that sets the stage for all of us now. I want to acknowledge the ongoing support of conference sponsors and Accellera Systems Initiative for their financial backing.

As you make your way to DVCon U.S. 2018, our conference “front door” is managed by MP Associates who has been the conference committee’s back office the past year to bring this full program to you. I want to thank them for all their work as well.

With that, I look forward to seeing many returning faces and meeting new attendees. I offer each and everyone one of you a hearty welcome to DVCon U.S. 2018! Let’s come and learn, exchange ideas and advance design and verification together.

General Chair, DVCon U.S. 2018
Registration Hours
Location: Bayshore Foyer
Monday, February 26 .......................... 7:30am to 7:00pm
Tuesday, February 27 ......................... 7:30am to 6:00pm
Wednesday, February 28 .................... 7:30am to 6:00pm
Thursday, March 1 ............................. 7:30am to 4:00pm

Expo Hours
Location: Bayshore Ballroom
Monday, February 26 .......................... 5:00pm to 7:00pm
Tuesday, February 27 ......................... 2:30pm to 6:00pm
Wednesday, February 28 .................... 2:30pm to 6:00pm

Parking Instructions
Overnight self-parking will be $13.00 per day/per car with no in and out privileges.
Daily self-parking will be $11.00 per day/per car with no in and out privileges.
Local attendees are to scan their parking ticket at the designated DVCon U.S. 2018 validation area (Bayshore Foyer). The scanner will beep 3 times to notify the attendee has validated their tickets at the group discounted rate.
There are two pay stations inside the hotel. One is located near the convention entrance (Bayshore Foyer) side. This machine accepts both cash and credit card. The second pay station is located near the guest elevators near the South Parking Lot. This machine accepts only cash.

DVCon Tutorials & Proceedings Distribution
DVCon Conference Papers and Tutorial presenter slides will be delivered electronically online via a username and password.
To access: http://proceedings.dvcon.org
Badge ID = Registration Number (on your badge)
Your Email = Email address used for registration
Please refer to your registration receipt to access the files you are eligible to view.

Wireless Information
Enjoy free Wi-Fi at DVCon! Connect to the Conference Wi-Fi via:
Wi-Fi SSID: DVCon2018
No Password Required

Social Media At DVCon
Follow @DVCon on Twitter and get hourly conference announcements.
Also, tweet #DVCon about your experience and highlights at the conference!
Don't miss DVCon on Facebook at facebook.com/DVCon.
Best Paper & Poster Voting
All Access, Conference Only and One-Day only registrants are entitled to vote for the “DVCon Best Paper and Poster” awards. The attendees are the judges! Enjoy the convenience of voting from your PC and mobile device:
1. Go to http://vote.dvcon.org
2. Vote on the papers and posters you have attended

Awards Presentation
Wednesday, February 28 | Location: Bayshore Ballroom | 5:00pm
Join us on the Exhibit Floor for the announcement of the 2018 award recipients!

DoubleTree Hotel Floor Plan
General Chair
Dennis Brophy
Mentor, A Siemens Business
8005 SW Boeckman Rd.
Wilsonville, OR 97070
503-685-0893
dennis_brophy@mentor.com

Past Chair
Yatin Trivedi
Aricent, Inc.
2580, N. First Street
San Jose, CA 95134
650-265-8031
ytrivedi@yahoo.com

Tutorial Co-Chair
Aparna Dey
Cadence Design Systems, Inc.
2655 Seely Ave., Bldg. 9
San Jose, CA, 95134
408-914-6503
aparna@cadence.com

Panel Chair
Vanessa Cooper
Verilab, Inc.
609 Castle Ridge Rd., Ste. 210
Austin, TX 78746
512-537-3136, ext. 7101
vanessa.cooper@verilab.com

Publicity/Marketing Chair
Barbara Benjamin
HighPointe Communications
7400 SE Milwaukie Ave. #412
Portland, OR 97202
503-209-2323
barbara@hipcom.com

Vice Chair
Ambar Sarkar, Ph.D.
NVIDIA
2 Technology Park Dr
Westford, MA 01886.
508-292-1681
ambars@nvidia.com

Program Chair
Tom Fitzpatrick
Mentor, A Siemens Business
18 Whistle Post Ln.
Groton, MA 01450
978-448-8797
tom_fitzpatrick@mentor.com

Poster Chair
Srivatsa Vasudevan
Synopsys, Inc.
Srivatsa.Vasudevan@synopsys.com

Accellera Representative & Finance Chair
Lynn Garibaldi
Accellera Systems Initiative
8698 Elk Grove Blvd. Ste 1, #114
Elk Grove, CA 95624
916-670-1056
Lynn@accellera.org

Conference Manager
Nannette Jordan
MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
303-530-4562
nannette@mpassociates.com
TECHNICAL PROGRAM COMMITTEE

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*Western Digital Corp.*

Kamel Belhous  
*Teradyne, Inc.*

Dan Benua  
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About Accellera Systems Initiative

Accellera Systems Initiative is an independent, not-for-profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other “smart” electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission
At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

• Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.

• Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.

• Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.

• Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.

• Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.

• Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

Membership
Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

Accellera Systems Initiative Technical Excellence Award

Accellera wishes to recognize the outstanding achievements of its Working Group members by selecting outstanding contributors to our standards development process as recipients of the Accellera Systems Initiative Technical Excellence Award.

This annual award recognizes major contributions to the development of Accellera standards. Examples of such contributions may include leadership in standardization of new technologies, assuring achievement of standards development goals, and identifying opportunities to better serve the needs of the community through standards.

Any member of an Accellera Working Group is eligible for the award. Candidates can be nominated by Working Group chairs and are endorsed and selected by participants of the Accellera Technical Excellence Award Committee, which is a subcommittee of the Technical Committee.

Past Recipients:
2017: Thomas Alsop, Intel
2016: Erwin de Kock
2015: Justin Refice
2014: Andrew Goodrich
2013: Janick Bergeron

For more information about Accellera awards programs and to find out how to submit a nomination, visit accellera.org/about/awards.
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Thank you to our Short Workshop Sponsors
Monday, February 26 Tutorials

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<td><strong>Coffee Break</strong></td>
<td><em>Gateway Foyer</em></td>
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| 9:00am - 12:00pm | **Tutorial 1**  
Portable Test and Stimulus: The Next Level of Verification  
Productivity is Here  
*Room: Oak/Fir* | |
| 12:00pm - 1:30pm | **Sponsored Luncheon**  
Accellera Lunch Featuring the 2018 Technical Excellence Award and  
Accellera Standards Activities  
*Room: Pine/Cedar* | |
| 2:00pm - 5:00pm | **Tutorial 2**  
IEEE-Compatible UVM Reference Implementation and Verification  
Components  
*Room: Oak/Fir* | |
| 3:00pm - 4:00pm | **Coffee Break**                                                      | *Gateway Foyer* |
| 5:00pm - 7:00pm | **DVCon Expo and Reception**  
*Room: Bayshore Ballroom*  
Cocktails and conversations in a casual environment with the DVCon exhibitors.  
Mingle from booth to booth while enjoying food and drinks. | |
Tutorial 1 - Portable Test and Stimulus: The Next Level of Verification Productivity is Here

Time: 9:00am - 12:00pm | Room: Oak/Fir

Organizer:
Tom Fitzpatrick - Mentor, A Siemens Business

Why reinvent the wheel? Up until now, verification teams had been unable to reuse tests as their efforts progressed from virtual platforms to RTL, block-level to system-level or from simulation to emulation, prototyping or silicon. The advent of UVM, constrained-random verification and functional coverage improved the reusability of portions of the verification environment, but these advances have not been able to enable reuse of verification intent throughout the product development process. Accellera formed the Portable Stimulus Working Group to produce a standard that would allow just this sort of verification intent reuse.

This in-depth technical tutorial will focus on a set of typical design use-cases from a variety of applications and show how to use the Portable Test and Stimulus Standard to create an abstract model of your verification intent. The tutorial will then demonstrate how these models can be used to generate scenarios to be executed on the different platforms and environments used in your development process, and how the models can be reused and leveraged from project to project.

For each application, we will show:
• How to model the critical verification intent,
• How that model may be used to generate multiple compatible coverage-centered scenarios,
• How to map that intent into multiple target-specific implementations,
• How the declarative semantics of the model drive the generation of executable tests on different platforms to implement the desired scenarios.

Speakers:
Faris Khundakjie - Intel Corp.
Tom Fitzpatrick - Mentor, A Siemens Business
Sharon Rosenberg - Cadence Design Systems, Inc.
Adnan Hamid - Breker Verification Systems, Inc.
Srivatsa Vasudevan - Synopsys, Inc.
Karthick Gururaj - Vayavya Labs Pvt., Ltd.

Thank you to our Sponsor:
Sponsored Luncheon - Accellera Lunch Featuring the 2018 Technical Excellence Award and Accellera Standards Activities

**Time:** 12:00pm - 1:30pm | **Room:** Pine/Cedar

Accellera Day 2018 at DVCon will be filled with exciting technical insights you’ll be able to apply immediately to your projects. In the middle of the day we’ll take a break and gather for lunch where we will have a presentation by Accellera that will include the 2018 Technical Excellence award, a look forward to the worldwide DVCon events, latest news, and working group activities. After that, we will have a panel of Accellera Working Groups Chairs giving brief updates on WG activities:

- **SystemC** – Trevor Wieman, *Intel and Frederic Doucet, Qualcomm*
- **SystemVerilog-AMS** – Peter Grove, *Dialog Semiconductor*

**Speakers:**
- **Trevor Wieman** - Intel Corp.
- **Peter Grove** - Dialog Semiconductor
- **Justin Refice** - Nvidia Corp.
- **Tom Fitzpatrick** - Mentor, A Siemens Business
- **Frederic Doucet** - Qualcomm, Inc.

Thank you to our Sponsor:

![Accellera Systems Initiative](image)

Tutorial 2 - IEEE-Compatible UVM Reference Implementation and Verification Components

**Time:** 2:00pm - 5:00pm | **Room:** Oak/Fir

**Organizer:**
Justin Refice - Nvidia Corp.

On April 11, 2017, the IEEE Standards Association (IEEE-SA) approved the IEEE 1800.2™ Standard for Universal Verification Methodology (UVM). For the tens of thousands of UVM verification engineers, this milestone connects teams to a standard recognized worldwide. However, the milestone does come with change. On one hand, there are many improvements and new features in the IEEE standard. On the other hand, there are changes to the both the standardized and undocumented APIs that many engineers accessed in the Accellera reference implementation to build their verification components.

This tutorial will introduce engineers to the new reference implementation aligned with IEEE 1800.2 created by the Accellera UVM WG. The speakers will use the new reference implementation to describe the new features and changes relative to UVM 1.2. Engineers attending the tutorial will learn the steps they need to take to update their verification components to be IEEE-compatible. Code examples and interactive discussions with members of the Accellera UVM WG will help engineers gain the practical knowledge they need to adopt the IEEE 1800.2™ Standard for UVM.

**Speakers:**
- **SystemRDL** – Steve Russell, *Zyzyx*
- **UVM** – Justin Refice, *Nvidia*
- **Portable Stimulus** – Tom Fitzpatrick, Mentor, A Siemens Business

**Speakers:**
- **Justin Refice** - Nvidia Corp.
- **Mark Strickland** - Cisco Systems, Inc.
- **Uwe Simm** - Cadence Design Systems, Inc.
- **Mark Peryer** - Mentor, A Siemens Business
- **Srivatsa Vasudevan** - Synopsys, Inc.

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<td>Session 3 Hardware Design Topics</td>
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<td>12:00pm - 1:15pm</td>
<td>Sponsored Luncheon Industry Leaders Verify with Synopsys</td>
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<td>Session 7 UVM 1: Registers and Integration</td>
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<td>5:00pm - 6:00pm</td>
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<td>6:00pm - 8:00pm</td>
<td>Colocated Event: Conquering Formal Verification: Go Deep or Go Broad?</td>
<td>Oak/Fir</td>
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Sponsored by: Synopsys
Opening Session

Time: 8:15am - 8:45am | Room: Oak

Join us as we set the stage for the 2018 DVCon Conference and Exhibition. DVCon's Steering Committee will highlight the conference’s events.

Session 1 - Clock Domain and Timing Challenges

Time: 9:00am - 10:30am | Room: Oak

Chair:
Josh Rensch - GLOBALFOUNDRIES

New techniques to solve clock domains and timing issues.

1.1 Clock Domain Crossing Challenges in Latch Based Designs
Madan M. Das, Chris Kwok, Kurt Takara - Mentor, A Siemens Business

1.2 Using Formal to Exhaustively Determine Unsafe Clock Ratios Between Asynchronous Blocks
Eric Hendrickson - NASA’s Jet Propulsion Lab
Bill Au, Joe Hupcey III, Richard Ilaca - Mentor, A Siemens Business

1.3 Leveraging More from GLS: Using Metric Driven GLS Stimuli to Boost Timing Verification
Sowmya Ega, Richardson Jeyapaul, Kunal Jani - Analog Devices, Inc.

Session 2 - Portable Stimulus Applications

Time: 9:00am - 10:30am | Room: Fir

Chair:
Ambar Sarkar - NVIDIA

Using Portable Stimulus in real applications.

2.1 Portable Stimulus vs Formal vs UVM: A Comparative Analysis of Verification Methodologies Throughout the Life of an IP Block
Gaurav Bhatnagar, David Brownell - Analog Devices, Inc.

2.2 Building Portable Stimulus Into Your IP-XACT Flow
Petri Karppa, Lauri Matilainen - Nokia
Matthew Ballance - Mentor, A Siemens Business

2.3 Bridge the Portable Test and Stimulus to UVM Simulation Environment
Theta Yang, Evean Qin - Advanced Micro Devices, Inc.
**Session 3 - Hardware Design Topics**

*Time: 9:00am - 10:30am | Room: Monterey/Carmel*

**Chair:**
Srivatsa Vasudevan - Synopsys, Inc.

What's new for hardware designers.

### 3.1 VHDL 2017: New and Noteworthy
*Lieuven Lemiengre, Hendrik Eeckhaut - Sigasi nv*

### 3.2 IDEs Should be Available to Hardware Engineers Too!
*Syed Daniyal Khurram, Horace Chan - Microsemi Corp.*

### 3.3 Automated Physical Hierarchy Generation: Tools and Methodology
*Ali S. El-Zein, Alvan Ng - IBM Corp.*
Benedikt Geukes - IBM Deutschland Research & Development GmbH
Maya Safieddine - IBM Corp.
Wolfgang Roesner - IBM Systems and Technology Group

**Poster Session 4 - Poster Session**

*Time: 10:30am - 12:00pm | Room: Gateway Foyer*

**Chair:**
Srivatsa Vasudevan - Synopsys, Inc.

### 4.1 Creating the Optimal Regression Farm Infrastructure That Meets All Your Team's Simulation Requirements
*David Lacey, Ed Powell - Hewlett Packard Enterprise*

### 4.2 Rockin' the Polymorphism for an Elegant UVM Testbench Architecture for a Scalable, Highly Configurable, Extensible DUT
*Michael Baird - Willamette HDL*
Frank Verhoorn - Northwest Logic Inc.

### 4.3 UVM-FM: Reusable Extension Layer for UVM to Simplify Functional Modeling
*Ahmed M. Ahmed Kamal - Mentor, A Siemens Business*

### 4.4 Unraveling the Complexities of Functional Coverage: An Advanced Guide to Simplify your use Model
*Thomas Ellis, Rohit Jain - Mentor, A Siemens Business*

### 4.5 Verification Strategy for Pipeline Type of Design
*Djuro P. Grubor - VTool Ltd.*

### 4.6 Sub-Design Interface Aware Top Only Low Power Verification
*Heichang Lee, Synopsys, Inc. & Samsung Electronics Co., Ltd.*
Nikhil Amin - Synopsys India Pvt. Ltd.
Jianfeng Liu, Minyoung Mo, Dongkwan Han - Samsung Electronics Co., Ltd.

### 4.7 A Specification-Driven Methodology for the Design and Verification of Reset Domain Crossing Logic
*Priya Viswanathan, Kurt Takara, Chris Kwok, Islam Ahmed - Mentor, A Siemens Business*

### 4.8 Context-Aware DFM Rule Analysis and Scoring Using Machine Learning
*Vikas Tripathi, Yongfu Li, I-Lun Tseng, Valerio Perez, Jonathan Ong, Zhao Chuan Lee - GLOBALFOUNDRIES*

### 4.9 Proper Probing: Flexibility on the TLM level
*Gergo Vekony - Almotive*

### 4.10 Holistic Approach to IO Timing Verification Using Portable Stimulus and Assertions
*Amitesh Khandelwal, Praveen Kumar - Infineon Technologies AG*

### 4.11 Managing and Automating Hw/Sw Tests from IP to SoC
*Matthew Ballance - Mentor, A Siemens Business*

### 4.12 Preventing Chip-Killing Glitches on CDC Paths with Automated Formal Analysis
*Jackie Hsiung - MediaTek, Inc.*
Ashish Hari, Sulabh K. Khare - Mentor, A Siemens Business
4.13 An Analytical View of Test Results Using Cityscapes
Markus Borg - SICS Swedish ICT
Andreas Brytting - KTH Royal Institute of Technology
Daniel Hansson - Verifyer AB

4.14 Reusable UPF: Transitioning from RTL to Gate Level Verification
Durgesh Prasad, Madhur Bhargava - Mentor, A Siemens Business, Jitesh Bansal - Mentor, A Siemens Business & Accenture Digital

4.15 Hybrid Approach to Testbench and Software Driven Verification on Emulation
Debdutta Bhattacharya, Ayub Khan - Mentor, A Siemens Business

4.16 Fast Track Formal Verification Signoff
Mandar Munishwar - Qualcomm, Inc.
Xiaolin Chen, Arunava Saha - Synopsys, Inc.
Sandeep Jana - Synopsys India Pvt. Ltd.

4.17 What Time Is It: Implementing a SystemVerilog Object-Oriented Wrapper for Interacting with the C Library time
Eldon G. Nelson - Synopsys, Inc.

4.18 Is Specman Still Relevant? Using UVM-ML to Take Advantage of Multiple Verification Languages
Timothy Pertuit, Doug Gibson, David Lacey - Hewlett Packard Enterprise

4.19 Formal Verification of Silicon for Software Defined Networking
Saurabh Shrivastava, Keqin Han - Cavium, Inc., Anh Tran - Cavium, Inc. & Xilinx, Inc.
Chirag Agarwal, Ankit Saxena, Anshul Jain, Achin Mittal, Roger Sabbagh - Oski Technology, Inc.

4.20 SoC Verification of Analog IP Integration through Automated, Formal-Based, Rule-Driven Spec Generation
Murugesh Palaniswamy, Ravi Kalyanaraman - Synopsys Incorporated
Gargi Sharma, Bharat Baliga-Savel - Mentor, A Siemens Business

Piyush Verma, Robert Pack, Robert E. Boone, Karthik Krishnamoorthy, Fadi Batarseh, Sriram Madhavan - GLOBALFOUNDRIES

4.22 UVM Testbench Design for ISA Functional Verification of a Microprocessor
Gabriel Wang, Hongtao Ma, Maoduo Sun - MediaTek, Inc.

4.23 SGEN2: Evolution of a Sequence-Based Stimulus Engine for Micro-Processor Verification
Stephan Bourduas, Christopher Mikulis - Cavium, Inc.

4.24 Synthesis of Decoder Tables Using Formal Verification Tools
Keethikumara Devarajegowda - Infineon Technologies AG & Technische Univ. Kaiserslautern
Johannes Schreiner, Wolfgang Ecker - Infineon Technologies AG & Technische Univ. Munchen

4.25 Ultimate Shift Left: Unleash the Power of UVM Virtual LAB Methodology upon SOC Verification
Roman Wang - Advanced Micro Devices, Inc.

4.26 Tired of Slow Gate Level Design Verification? Use these Efficient Modelling Styles and Methodology
Rohit Jain, Shobana Sudhakar - Mentor, A Siemens Business

4.27 Making Security Verification “SECURE”
Subin Thykkoottathil, Nagesh N. Ranganath - Analog Devices, Inc.

4.28 Don’t Delay Catching Bugs: Using UVM Based Architecture to Model External Board Delays
Amit Paunikar, Saurabh Arya, Vikas Makhija, Shaily Khare - Synopsys India Pvt. Ltd.

4.29 Comprehensive IP to SoC Clock Domain Crossing Verification Using Hybrid Data Model
Anwesha Choudhury, Ashish Hari - Mentor, A Siemens Business

4.30 Cleaning Out Your Pipes - Pipeline Debug in UVM Testbenches
Rich Edelman - Mentor, A Siemens Business
Neil Bulman - ARM Ltd.

4.31 Improving Verification Predictability and Efficiency Using Big Data
Darron K. May - Mentor, A Siemens Business
Sponsored Luncheon - Industry Leaders Verify with Synopsys

**Time:** 12:00pm - 1:15pm  |  **Room:** Pine/Cedar

**Moderator:**
Piyush Sancheti - Synopsys, Inc.

Synopsys has partnered with industry leaders to define and deploy breakthrough technologies that not only increase the speed and throughput of SoC verification but also offer innovative approaches to avoid bugs altogether, detect them as early as possible, debug more efficiently, and enable early software bring-up. At this luncheon, you will hear industry experts share their viewpoints on what is driving SoC complexity, how their teams have achieved success, how you can apply their insights on your next project as well as discussions about the latest developments in the verification landscape and advanced technology.

**Panelists:**
- Deepak Manoharan - Qualcomm, Inc.
- Brian Fisk - Advanced Micro Devices, Inc.

Thank you to our Sponsor:

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Keynote: Industry’s Next Challenge: The Petecycle Challenge

**Time:** 1:30pm - 2:30pm  |  **Room:** Oak/Fir

**Speaker**
Christopher Tice - Synopsys, Inc.

This keynote highlights how new growth segments in the industry, such as Automotive, IoT, Networking, 5G Mobile, etc. are fundamentally changing the requirements for verification. The keynote will emphasize how addressing the SoC verification, software bring-up and validation needed for these segments will change the nature of verification technologies and solutions.

**Biography:** Christopher Tice is vice president of Verification Continuum Solutions in the Verification Group, responsible for driving the growth of Synopsys’ verification business based on a foundation of solutions addressing fast-growing verticals such as automotive, networking, and IoT.

Before joining Synopsys, he was an entrepreneur-in-residence at SK Telecom Innopartners. Mr. Tice spent 16 years at Cadence Design Systems where he was senior vice president and general manager of the Hardware and Systems Groups. Prior roles included vice president of Quickturn Design Systems and general manager of Weitek's Processor Business Group. Mr. Tice received his BSEE with honors from the University of Florida and attended the MBA School at Florida Atlantic University. He was elected as an inaugural member of the Electrical and Computer Engineering Academy of the University of Florida in 2009.
Session 5 - Emulation Use Models

Time: 3:00pm - 4:30pm | Room: Oak

Chair:
Kamel Belhous - Teradyne, Inc.

Including emulation in your verification flow.

5.1 Transparenl Checkpointing Software Test Benches to Improve Productivity of SoC Verification in an Emulation Environment
Ankit Garg, Suresh Krishnamurthy - Mentor, A Siemens Business
Gene Cooperman, Rohan Garg - Northeastern Univ.
Jeff Evans - Mentor, A Siemens Business

5.2 UVM Acceleration Using Hardware Emulator at Pre-Silicon Stage
Sunil Roe - Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc.
YunGi Um, Hyunwoo Koh, Hyunsun Ahn, Youngsik Kim, Seonil Brian Choi - Samsung Electronics Co., Ltd.

5.3 UVM-Based Verification of a RISC-V Processor Core Using a Golden Predictor Model and a Configuration Layer
Marcela Zachariasova, Lubos Moravec - Codasip Ltd.
John Stickley, Hans van der Schoot, Shakeel Jeeawoody, Ritesh Goel - Mentor, A Siemens Business

Session 6 - Improving Coverage

Time: 3:00pm - 4:30pm | Room: Fir

Chair:
Dave Rich - Mentor, A Siemens Business

New approaches in coverage modeling and analysis.

6.1 Deep Predictive Coverage Collection
Rajarshi Roy, Chinmay Duvedi, Saad Godil, Mark Williams - Nvidia Corp.

6.2 Debugging Functional Coverage Models get the Most out of Your Cover Crosses
Mennatallah Amer, Amr A. Hany - Mentor, A Siemens Business

6.3 Automated Seed Selection Algorithm for an Arbitrary Test Suite
David Crutchfield, Brandon Skaggs, Brian Craw, Jim Sharpe - Cypress Semiconductor Corp.
Colocated Meeting - Conquering Formal Verification: Go Deep or Go Broad?

**Time:** 6:00pm - 8:00pm  |  **Room:** Oak/Fir

**Moderator:**
Sean Safarpour - Synopsys, Inc.

Successful users of formal verification often fall into one of two camps: The deep Property Verification advocates and the Broad Formal Apps advocates. In terms of impact on the verification cycle - reducing verification time/effort and finding more bugs - which approach has been most successful: doing deep verification with custom-written assertions often by formal experts OR the application of formal Apps such as Connectivity Checking, Unreachability Analysis or Register Verification to name a few. While going deep is often very powerful, it is limited to experts who can use it effectively. On the other hand, going broad can be used by thousands of engineers with minimal training, but the impact is limited to existing off-the-shelf applications. A panel of passionate verification engineers and managers join us to share their perspective of the most successful deployment of formal verification.

**Evening Agenda:**

6:00 – 6:30pm: Appetizers, drinks and socializing, + Formal Challenge
6:30 – 7:30pm: Panel
7:30pm: Puzzle winner announcement
7:30 – 8pm: Dessert, drinks and socializing

**Panelists:**
- **Erik Seligman** - Intel Corp.
- **Naveed Zaman** - Qualcomm, Inc.
- **Shaun Feng** - Samsung Semiconductor, Inc.
- **Vigyan Singhal** - Oski Technology, Inc.
- **Ashish Darbari** - Axiomise Ltd.

**Please note:** DVCon Conference Badge required for entrance.

**Sponsored by:** Synopsys
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<td><strong>DVCon Reception</strong></td>
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Panel: Help! System Coverage is a Big Data Problem!

*Time: 8:30am - 9:30am | Room: Oak/Fir*

**Moderator:**
Brian Bailey - *Semiconductor Engineering*

**Organizers:**
Maheen Hamid - *Breker Verification Systems, Inc.*
Dave Kelf - *Breker Verification Systems, Inc.*

While coverage is undergoing a renaissance, partly driven by new automotive systematic verification methodologies that demand a rigorous approach to measuring system coverage versus original specification, more attention to system coverage is needed.

Coverage metrics help development groups understand the quality of their verification efforts and coverage holes represent risk of failure. At the system level, there are no standardized metrics and no way to exhaustively close coverage. The emergence of Portable Stimulus brings some structure to the problem, but opens up as many questions as it provides answers. For a typical design, the total number of paths through a graph is on the order of 2100 and that's before all the possible concurrency issues are considered.

System coverage has all of the hallmarks of being a big data problem.

The good news is that system coverage is directly tied to intent and development groups soon will have better quality metrics than they did in the past.

Moderator Brian Bailey and a panel of experts will explore various best practices in use by the industry. They will examine ways in which Portable Stimulus, formal verification methods, emulation and prototyping can be used to help provide the necessary confidence.

**Panelists:**
- **Vigyan Singhal** - Oski Technology, Inc.
- **Mark Glasser** - Nvidia Corp.
- **Mike Bartley** - Test and Verification Solutions
- **Adnan Hamid** - Breker Verification Systems, Inc.
- **Ashish Darbari** - Axiomise Ltd.

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**Session 8 - UVM 2: Use Models**

*Time: 10:00am - 12:00pm | Room: Oak*

**Chair:**
Greg Tumbush - *Tumbush Enterprises, LLC*

Applications of UVM to solve challenging problems

8.1 **UVM for HLS: An Expedient Approach to the Functional Verification of HLS Designs**
*Dave Burgoon,* Robert Havlik - *Microsoft Corp.*

8.2 **Common Challenges & Solutions to Integrating a UVM Testbench in Place of a Legacy Monolithic Testing Environment**
*Frank Verhoorn* - *Northwest Logic Inc.*
Michael Baird - *Willamette HDL*

8.3 **UVM and C Tests - Perfect Together**
*Rich Edelman* - *Mentor, A Siemens Business*

8.4 **UVM Verification Environment Based on Software Design Patterns**
*Darko M. Tomusilovic,* Hagai Arbel - *VTool Ltd.*
Session 9 - Formal Verification Use Models

Time: 10:00am - 12:00pm | Room: Fir

Chair:
Harry Foster - Mentor, A Siemens Business

Applying formal verification to challenging system-level problems.

9.1 An Efficient and Modular Approach for Formally Verifying Cache Implementations
Achutha Kiran Kumar V. Madhunapantula - Intel Corp.
Abhijith A. Bharadwaj - Intel Technology India Pvt. Ltd.
Bindumadhava S. Singanamalli - Intel Corp.
Erik Seligman - Intel Corp.

9.2 Architectural Formal Verification of System-Level Deadlocks
Mandar Munishwar, Naveed Zaman - Qualcomm, Inc.
Anshul Jain, HarGovind Singh, Vigyan Singhal - Oski Technology, Inc.

9.3 Formal Architectural Specification and Verification of a Complex SoC
Shahid Ikram, Isam Akkwai, David Asher, Jim Ellis - Cavium, Inc.

9.4 Formal Verification of Connections at SoC-level
Penny Yang - Synopsys Taiwan Co., Ltd.
Prasun Das - Synopsys India Pvt. Ltd.
Yuya Kao, Mingchu Kuo - MediaTek, Inc.

Session 10 - Solving Reuse Challenges

Time: 10:00am - 12:00pm | Room: Monterey/Carmel

Chair:
John Dickol - Samsung Austin R&D Center

Practical approaches to simplifying the art and science of Reuse.

10.1 Practical Scheme to Enhance Verification Turn-Around-Time by Using Reusable Harness Interface (RHI)
Jong pil Jung, Hyunju Lee, Jaejin Ha, Yonghee Im - SK hynix Inc.

10.2 Challenges and Mitigation’s of Porting a UVM Testbench from Simulation to Transaction-Based Acceleration (Co-Emulation)
Vikas Billa, Sundararajan Haran - Microsemi Corp.
*Previously presented at DVCon India 2017

10.3 IP-XACT based SoC Interconnect Verification Automation
Youngrae Cho, Youngsik Kim, Seonil Brian Choi - Samsung Electronics Co., Ltd.

10.4 Managing Highly Configurable Design and Verification
Jeremy Ridgeway - Broadcom Limited
Sponsored Luncheon - Validation: Verification’s Big Brother
- “I Wanna Go Fast”

Time: 12:00pm - 1:15pm | Room: Pine/Cedar

Speakers:
Stephen Bailey - Mentor, A Siemens Business
Doug Amos - Mentor, A Siemens Business

Verification & Validation Methodology for Acceleration
Achieving the highest productivity in the number of cycles requires a methodology to create environments and tests that enable the best performance from simulation, emulation and prototyping while also enabling the use of the best engines for the verification and validation objective without requiring changes to your environment and test IP. Come join us for food for your body and nourishing ideas for your high productivity verification & validation brain.

Thank you to our Sponsor:

Mentor
A Siemens Business
Panel: The Right Tool (or Tools) for the Toughest Verification Tasks

*Time: 1:30pm - 2:30pm | Room: Oak/Fir*

**Moderator:**
Jean-Marie Brunet - Mentor, A Siemens Business

**Organizer:**
Nanette Collins - Nanette V. Collins Marketing and Public Relations

Emulation, simulation, formal verification and FPGA prototyping, along with a mix of methodologies, are often evaluated by verification groups to assess their ability to solve every conceivable verification challenge.

Some verification groups tout emulation as the primary verification technology as simulation reaches its outer limits and FPGA prototyping is consigned to smaller designs. They now consider emulation to be among the most capable tools to meet their challenging chip design verification requirement through better reliability, more use models and greater flexibility.

Of course, the verification checkerboard benefits from the adoption of formal verification as it too has more use models and a significant number of expert users. Accellera’s Portable Stimulus standard could play some role in the future, predicts a handful of verification engineers.

New developments on the verification front promise to fuel a fascinating discussion among panelists who will describe how decisions are made about which tools are implemented in a design verification flow. And how budgets are allocated. As users, they will explain why some tools dominate today’s flow and others not so much.

**Panelists:**
- Suman K. Mandal - Intel Corp.
- Bill Neifert - ARM Ltd.
- Alex Starr - Advanced Micro Devices, Inc.
- Guy Hutchison - Cavium
- Nasr Ullah - Samsung Austin R&D Center

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**Session 11 - Formal and Assertion-Based Verification**

*Time: 3:00pm - 4:30pm | Room: Oak*

**Chair:**
Dan Benua - Cadence Design Systems, Inc.

Interesting applications of assertion-based and formal verification.

**11.1 Formal Verification on Deep Learning Instructions of GPU**
Jian (Jeffrey) Wang, Jia Zhu - Advanced Micro Devices, Inc.

**11.2 Let’s be Formal while Talking About Verification Quality: A Novel Approach to Qualify Assertion based VIPs**
Sachin Scaria, Surinder Sood - Intel Technology India Pvt. Ltd
Erik Seligman - Intel Corp.

**11.3 Formal Verification of Floating-Point Hardware with Assertion-Based VIP**
Sasa Stamenkovic - OneSpin Solutions GmbH
Ravi Ram, Adam Elkins, Adnan Pratama - Xilinx Inc.
Sven Beyer, Sergio Marchese - OneSpin Solutions GmbH
Session 12 - Safety-Critical Verification

Time: 3:00pm - 4:30pm | Room: Fir

Chair:
Clifford Cummings - Sunburst Design, Inc.

Using automation and advanced techniques to meet safety requirements.

12.1 Whose Fault Is It Formally? Formal Techniques for Optimizing ISO 26262 Fault Analysis
Ping Yeung, Doug Smith, Abdelouahab Ayari - Mentor, A Siemens Business

12.2 Using Automation to Close the Loop Between Functional Requirements and Their Verification
Brian Craw, David Crutchfield, Martin Oberkoenig, Markus Heigl, Martin O'Keeffe - Cypress Semiconductor Corp.

12.3 Error Injection in a Subsystem Level Constrained Random UVM Testbench
Jeremy Ridgeway, Hoe Nguyen - Broadcom Limited

Session 13 - Verifying Low-Power Designs

Time: 3:00pm - 4:30pm | Room: Monterey/Carmel

Chair:
Logie Ramachandran - VeriKwest Systems Inc.

The latest techniques for low-power verification.

13.1 Unveil the Mystery of Code Coverage in Low-Power Designs: Achieving Power Aware Verification Closure
Madhur Bhargava, Durgesh Prasad - Mentor Graphics (India) Pvt. Ltd.
Pavan Rangudu - Mentor, A Siemens Business

13.2 Low Power Coverage: The Missing Piece of Dynamic Simulation
Progyna Khondkar, Ping Yeung, Gabriel Chidolue - Mentor, A Siemens Business

13.3 Low Power Apps: Shaping the Future of Low Power Verification
Awashesh Kumar, Madhur Bhargava, Pankaj Gairola, Vinay K. Singh - Mentor Graphics (India) Pvt. Ltd.

Best Paper & Poster Awards Presentation

Time: 4:45pm - 5:00pm | Room: Bayshore Ballroom

2018 Recipients of the Best Paper and Poster are announced by Technical Program Chair, Tom Fitzpatrick.
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THURSDAY’S AGENDA

8:00am - 11:00am
Coffee Break
Room: Gateway

8:30am - 10:00am
Short Workshop 1
Deep Learning for Design and Verification Engineers
Room: Sierra

8:30am - 12:00pm
Tutorial 3
SoC Verification Speed – More is Better
Room: Donner

Tutorial 4
Comprehensive Metrics-Based Methodology to Achieve Low-Power System-on-Chips
Room: Siskiyou

Tutorial 5
Formal Verification – Breaking Through the Knowledge Barrier
Room: Cascade

10:30am - 12:00pm
Short Workshop 2
Formal Verification in the Real World
Room: Sierra

12:15pm - 1:45pm
Sponsored Luncheon
Smarter and Faster Verification: Beyond Brute Force
Room: Cascade/Sierra

2:00pm - 3:30pm
Short Workshop 3
Using Mutation Coverage For Advanced Bug Hunting
Room: Sierra

2:00pm - 5:30pm
Tutorial 6
Making Cars Safer - One Chip at a Time
Room: Donner

Tutorial 7
How to Stay Out of the News with ISO26262-Compliant Verification
Room: Siskiyou

Tutorial 8
Functional Safety Verification for ISO 26262-Compliant Automotive Designs – What’s New and What’s Needed
Room: Cascade

3:30pm - 4:00pm
Coffee Break
Room: Gateway

4:00pm - 5:30pm
Short Workshop 4
Just Do It. Users Want Results, not Technology. Who Cares if a Structural Analysis Tool is Using Formal Verification?
Room: Sierra
Short Workshop 1 - Deep Learning for Design and Verification Engineers

Time: 8:30am - 10:00am | Room: Sierra

Organizer:
John Aynsley - Doulos Ltd.

Deep learning is a very hot topic right now. The success of deep learning algorithms in the ImageNet Large Scale Visual Recognition Challenge (ILSVRC) has brought deep learning to everyone’s attention. Although deep learning does of course get over-hyped, its effectiveness in the wider context of machine learning and data science is undeniable. Deep learning algorithms are proving effective in many existing applications such as image recognition, speech recognition, and natural language processing. Deep learning algorithms are opening the door to many totally novel applications and products, from smart homes to autonomous vehicles, from defense systems to medical systems.

Deep learning will impact D&V engineers in a number of ways, from the kinds of electronic product we design and verify through to the algorithms used within design and verification tools. Last year we saw machine learning papers starting to appear at DVCon.

This workshop gives a basic introduction to the subject of deep learning specifically aimed at the interests and the skill set of the design and verification engineers who comprise the DVCon audience. The workshop explains the background to deep learning, the technical jargon, and the main concepts you need to get started. Topics to be covered include basic machine learning algorithms for regression and classification, cost functions, basic neural network models, the distinction between machine learning and deep learning, the training and deployment of neural network models, an overview of the ecosystem including common deep learning software libraries and frameworks, and how to get started with deep learning. The workshop includes access to working code examples and instruction on how to run them yourself.

Speaker:
John Aynsley - Doulos Ltd.

Thank you to our Sponsor:
The title is cliché unless you are already neck-deep in SoC verification. Sure, the casual observer knows that making any verification engine faster will speed-up verification closure. That is a foundation statement that can't be taken for granted because achieving it requires advanced engineering. But SoCs are more complex than the lines of RTL that describe them. They mix new and reused designs. The have untimed models above RTL. They have analog, power, software, and safety IP. They have directed, randomized, software driven, and real-world test. More speed in a given engine is better, but more fast engines and more unified engines is better as well.

For this tutorial, we'll add another more – more depth – to dig into how these engines can be used to enhance SoC verification speed. Starting with formal, we'll examine how to apply new formal engines and apps to speed IP verification and key SoC verification tasks. In simulation, we'll walk through examples of how maximize individual test and farm performance for high-volume tests and then how to do the same for long-latency tests in pure digital and low-power/mixed-signal designs. We will then create the high-performance test bridge from software to hardware engines verification by applying production-proven portable stimulus. We’ll then continue the verification with acceleration, emulation, and FPGA prototyping solutions that maximize both bring-up and runtime performance. Speed, speed, and more speed.

In fact, all of this speed can be summarized as “Mores” Law for verification. Not the Moore’s Law for design which describes geometrically growing design task, but a new one that addresses the exponentially growing task of verification. This law demands that you have a broad knowledge of the engines and methods needed to squeeze more verification speed into your project. When you attend this tutorial, you'll get more practical knowledge from technology experts that you can immediately apply. More is better.

Speakers:

- **Fernanda Braga** - Cadence Design Systems, Inc.
- **John Rose** - Cadence Design Systems, Inc.
- **Sharon Rosenberg** - Cadence Design Systems, Inc.
- **Frank Schirrmieister** - Cadence Design Systems, Inc.
- **William Winkeler** - Cadence Design Systems, Inc.

Thank you to our Sponsor: *cadence*
Tutorial 4 - Comprehensive Metrics-Based Methodology to Achieve Low-Power System-on-Chips

Time: 8:30am - 12:00pm | Room: Siskiyou

Organizer:
Rebecca Granquist - Mentor, A Siemens Business

Driven by process technology needs, government legislation, and continued product integration and miniaturization, reducing power consumption is a mainstream and essential design requirement for many industry segments; including networking, mobile, automotive, consumer, and IoT.

Because of this, many designs now employ sophisticated power management techniques. For example, design teams implement more power domains per design where each power domain can be placed in many different power states. Unfortunately though, most project managers lack a standard metric for power verification, and because of this do not know how well power management is verified.

Besides using power management techniques, design teams are also trying to reduce their power in the RTL design process by reducing unnecessary switching activity. This process can be difficult and the ultimate effect from RTL modifications are hard to predict.

Lastly, to get a comprehensive methodology for both power measurement and power reduction, it is important to have realistic and accurate switching scenarios for particular power modes. Again, these can often be difficult to create and depend on very large datasets to drive verification results.

In this tutorial, we will step through a complete low-power methodology, and explore the different types of metrics needed at different phases of the design process. It will cover a new and unique low-power coverage methodology that enables designers to verify and track how well they have tested their power management architecture. It will also show how to track not only metrics for how much power is used in the RTL, but also how much power is still being wasted and has potential to be reduced for IP qualification. Finally, it will step through how to bring real power scenarios testing into both your power measurement and management coverage metrics to provide the final phase of power verification and validation.

Speakers:
Ellie Burns - Mentor, A Siemens Business
Gabriel Chidolue - Mentor, A Siemens Business
Guillaume Boillet - Mentor, A Siemens Business

Thank you to our Sponsor:
Tutorial 5 - Formal Verification - Breaking Through the Knowledge Barrier

**Time: 8:30am - 12:00pm | Room: Cascade**

**Moderator:**
Sean Safarpour - Synopsys, Inc.

**Organizer:**
Kiran Vittal - Synopsys, Inc.

Formal Verification has become a mainstream verification technology and methodology. Over the previous two decades, early adopters paved the way to demonstrate how formal verification can improve quality and timelines by catching more bugs faster and with higher confidence. While the technology itself is deployed at many hundreds of companies in the form of property verification, bus protocol verification, connectivity checking, coverage closure and many other applications, there are still relatively few design or verification engineers who get the maximum value out of formal verification. The reason for this productivity gap is that advanced formal verification knowledge acquired over dozens of projects and many years is not readily accessible to the general public and limited to the confinies of the experts.

In this tutorial, the top-most industry leaders in formal verification attempt to break the knowledge barrier. They will introduce, teach and provide detailed analysis on some of the most advanced formal verification techniques.

Topics covered are:

- Describe abstraction both from a concept and practical perspective. Walk through case studies and describe the impact of this technique on getting proofs and unearthing deep bugs.

- How to efficiently verify blocks with common but dreaded data structures such as such as FIFOs, RAMs and caches with formal verification along with concept of symbolic variables

- How to effectively close inductive-based proofs with invariants. This technique is very powerful in getting full proofs for certain types of properties, although few are aware of how to use it.

- How to sign-off complex blocks entirely with formal verification. Unearth short comings in terms of assertions and verification holes in over-constraint analysis

- How to perform Architectural Formal Verification to prove correctness of Coherency Models. Coherency is a key requirement of a multi-processor system and it is of utmost importance to the functionality of the design. Usage of stale data due to bugs in implementation of coherency protocol may result in illegal behavior.

Armed with this knowledge, verification engineers will be able to improve their overall efficiency with formal verification.

**Speakers:**

- **Shaun Feng** - Samsung Austin R&D Center
- **Syed Suhaib** - Nvidia Corp.
- **Mandar Munishwar** - Qualcomm, Inc.
- **Iain Singleton** - Synopsys, Inc.

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Building on our well-received foundation-level tutorial Formal Verification – Too Good to Miss presented at DVCon Europe 2016, this session will cover some of the more advanced techniques and workflow patterns that have proven valuable in our own formal verification work.

Carefully avoiding mathematical jargon, it aims to demystify some approaches that help to make a formal verification project productive. Black-boxing, using abstractions for counters and other common structures, and exploiting design symmetry are often mentioned, but rarely described in an accessible way. They will all be covered in a practical style, emphasising broad applicability.

In addition to purely technical content, the session will illustrate how to approach the planning and tracking of your formal verification project – concerns that are easily overlooked in the initial enthusiasm of adopting formal.

This tutorial is appropriate for engineers who are embarking on, or part-way through, a project that uses formal verification. It tackles troublesome questions that commonly become challenges for anyone as their experience deepens: how to establish metrics and criteria for project progress, knowing when you’re done, overcoming performance and capacity issues, achieving confidence in the robustness and trustworthiness of your formal verification environment, and integrating results from formal into your simulation-based verification flow.

Speaker:

Jonathan Bromley - Verilab Ltd.

Thank you to our Sponsor:
Sponsored Luncheon - Smarter and Faster Verification: Beyond Brute Force

Time: 12:15pm - 1:45pm | Room: Cascade/Sierra

Moderator:
Frank Schirrmeister - Cadence Design Systems, Inc.

Organizer:
Larry Melling - Cadence Design Systems, Inc.

Over the past decade, the core engines of functional verification have matured. Formal verification, simulation, emulation and FPGA based prototyping are the core anchors to deliver verification productivity. While they continue to evolve and differentiate on core parameters like performance, capacity, memory footprint, the next leaps in productivity will be added in the fabric that binds them together with advanced analytics of the data created by the core engines. What will fuel these leaps?

Will it be smarter management of the engines?
- Switching between engines to leverage advantages and availability
- Selection of best engine for the task
- Optimizing engine use for overall throughput or latency

Will it be smarter testing?
- Good cycles vs. Bad cycles
- Which tests should be run more and which run less and with what parameters/setting?
- Which tests give highest return

Or will it be something else or all of the above?

It is safe to say that one thing all of these have in common is the need for relevant data that can be analyzed, correlated, and ranked.

This panel will review the requirements for verification in an increasingly application specific and connected world and examine the key trends in verification productivity and what impact data analytics and machine learning could have.

Panelists:
Mike Stellfox - Cadence Design Systems, Inc.
David Lacey - Hewlett Packard Enterprise
Seonil Brian Choi - Samsung Electronics Co., Ltd.

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Modern verification methodologies incorporate multiple coverage solutions. These range from functional to structural coverage, leverage various coverage models and operate using varied technologies in both the simulation and formal process.

The main purpose of these coverage solutions is to establish a signoff metric that indicates when enough verification has been performed. However, as coverage approaches have evolved, new use models have emerged for these tools that increases their value in the verification process. The ability of these tools to provide guidance to areas insufficiently tested, or uncover buggy scenarios is still being explored, to great effect.

Mutation coverage is a relatively new technique pioneered by formal and simulation providers. The approach is to pose the question: if my design is fully covered by a specific testbench or assertion set, then if I change something in the design, the tests should detect this change. If it doesn't then the area of change is not covered. Now if all the code segments across a block are changed, one by one, a very precise coverage metric may be established.

Of course, how the design is changed, or mutated, and how these mutations are implemented has a dramatic affect on the effectiveness and performance of the solution, but the approach is widely regarded as a highly effective method for establishing both structural and functional coverage, and is used in design flows where high degrees of coverage are mandatory.

Leveraging this mutation technique with formal tools provides some significant technology benefits, which accelerates the operation of the tool. In addition, the exhaustive nature of formal further improves the precision of the established coverage metric and allows for useful information on the source of uncovered scenarios to be obtained.

The performance and informative nature of formal-based mutation coverage has opened up a new use model in the area of bug hunting, where the tools may be used to analyze complex operational scenarios and detect extremely well hidden error conditions, otherwise hard-to-find using more traditional solutions.

This tutorial will focus on this bug hunting process. Leveraging a classic case study notorious for complex bugs, the attendees will be guided through a range of techniques applicable to many design applications, and shown how unusual bugs can manifest themselves and be detected using this technique.

The workshop agenda will consist of:
- Introduction to mutation coverage techniques
- Mutation coverage with formal – it's not so tough!
- Sign-off with mutation coverage
- Overview of bug hunting techniques with formal
- Bug hunting using mutation coverage
- Bug hunting on a practical design example
- Overview of potential improvements using this technique

Speakers:
Muhammad Haque Khan - OneSpin Solutions GmbH
Vladislav Palfy - OneSpin Solutions GmbH
Tutorial 6 - Making Cars Safer - One Chip at a Time

*Time: 2:00pm - 5:30pm | Room: Donner*

**Organizer:**
Ann Keffer - Cadence Design Systems, Inc.

Autonomous driving is real. Coming out of the realm of research, autonomous vehicles are now on roads around you. These vehicles integrate complex sensor data in real time to maintain their lane, keep a safe driving distance from other vehicles, brake for obstacles in the road, and much more. As engineers, we understand that these capabilities are built from sophisticated electronics, software, and mechanical system. But there is more to a safe vehicle than one tested to operate properly on purchase. Safe vehicles need to remain safe throughout their operating lifetime which means they need to not only operate safely but also need to fail safely.

These two elements mean that the electronics in safe vehicles need to be designed with both functional circuits, for planned operation, and detection circuits, for unplanned failures. This implies that safe electronics require two forms of verification: positive and negative. Positive verification tests that the overall design responds properly to both good and erroneous input. Negative verification tests that the overall design can detect errors in itself.

Achieving compliance to ISO 26262 requires a measurement of the extent to which both forms of verification have been completed. For engineers accustomed to traditional positive verification, the requirements for ISO 26262 compliance may require more rigorous methodologies than designs that don’t need safety compliance. Moreover, negative verification may require completely new tools and methodologies. This tutorial will explore the challenges in making autonomous vehicles safer and provide attendees with technical guidance they can use to implement the new methodologies they need to achieve compliance for their autonomous driving electronics.

**Speakers:**
Ann Keffer - Cadence Design Systems, Inc.
Apurva Kalia - Cadence Design Systems, Inc.

Tutorial 7 - How to Stay Out of the News with ISO26262-Compliant Verification

*Time: 2:00pm - 5:30pm | Room: Siskiyou*

As the transportation industry continues to increase the amount of electronics and embedded software included in its products, systems and semiconductor makers must now consider the fault tolerance of their product offerings to customers in this rapidly growing market. Fortunately, the ISO 26262 standard defines the safety level of a design via specific safety goals, safety mechanisms, and fault metrics. However, even though there are sections of ISO 26262 dedicated to electronic systems in general, and semiconductors in specific, the mapping of the specification to the implementation of design and verification best practices is not specifically delineated.

Hence, in this tutorial you will learn:

- How to estimate the safety level of a design by defining safety goals, selecting “safety mechanisms”, and specifying fault metrics
- How today’s dynamic, static, and hardware-assisted verification flows can be employed to verify the safety-critical RTL designs, gate-level implementations, and embedded bare-metal software and firmware
- Advanced techniques to eliminate large numbers of irrelevant faults without compromising the completeness of the verification, or the safety of the finished product

**Speakers:**
Doug Smith - Mentor, A Siemens Business
Charles Battikha - Mentor, A Siemens Business

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Tutorial 8 - Functional Safety Verification for ISO 26262-Compliant Automotive Designs - What’s New and What’s Needed

Time: 2:00pm - 5:30pm | Room: Cascade

Automotive has evolved into one of the fastest growing parts of the worldwide semiconductor industry, and automotive semiconductor content is exploding, driven by the LED headlights to the many advanced SoCs powering autonomous drive, infotainment, and vehicle communication systems. The “traditional” automotive electronics are not standing still either, with advanced drivetrains and sophisticated safety and ADAS systems creating demand for even-larger and more integrated SoCs.

As automotive electronic systems become ever more complex, the potential impact on the safety of vehicle’s occupants and bystanders becomes a critical consideration for these systems. ISO 26262, the functional safety standard for road vehicles was created to guide the development of electrical and electronic systems for automobiles, and meeting ISO 26262 compliance needs are rapidly becoming a part of many companies' design and verification requirements. For IP and SoC companies, ISO 26262 product development at the hardware level guidelines are particularly important—from a verification perspective, it lays out a set of requirements for functional safety that need to be understood and followed, and which are in addition to best-practice functional verification methodologies.

State-of-the-art functional safety verification is necessary, but not sufficient for ISO 26262. Functional verification seeks to find and eliminate design-related bugs, which would manifest as systematic faults during product operational lifecycles. In addition, complete functional safety verification must also be performed, with the objective of determining the product’s ability to safely manage random faults that may arise during its lifecycle. This is a different verification objective compared to functional verification, and is based on fault injection flows in addition to logic simulation flows.

This tutorial will provide a practical, hands-on overview of the following:

- ISO 26262 considerations for SoC and IP design verification, customer insights and today's challenges
- Unique challenges for automotive SoC and IP verification engineering teams
- New functional verification challenges, solutions and flows
- Functional safety verification
- Failure mode analysis
- Fault injection testing: best practice methodologies for verification engineers
- Annotation of diagnostic data
- Conclusions and QA

Speakers:

- Kevin Rich - Nvidia Corp.
- Meirav Nitzan - Synopsys, Inc.
- Shekhar Mahatme - Synopsys, Inc.
- Brian Davenport - Synopsys, Inc.

Thank you to our Sponsor: Synopsys
Formal Verification (FV) has crossed the chasm, in today's world, FV is simply another tool in the Electronic Design Automation (EDA) company's toolbelt for solving problems. You can effectively use an opensource FV engine on your hardware design, set the assertions, and query the engine for proofs that do (or don't, depending on the type of assertion) meet the expectations for success. This is no different, then in the '80s and '90s when everyone used Berkley's Binary Decision Diagram analysis engine for Boolean optimization. The problem is, since the 80's and 90's EDA has really become ED. We as EDA software developers and companies producing code, have removed more and more of the automation, and instead have highlighted our latest and greatest technology. EDA Vendors give the keys to the new technology to the users, and then turn around and charge them for consulting services when the tool takes forever to finish. This is not automation, its simply Electronic Design. This loss of `A'utomation in EDA is not new, but has been seeing a comeback with static analysis tools.

In the 90's Synplicity pushed automation into synthesis. Push a button get your gate level netlist, optimized appropriately. Users no longer had to decide from 10 different optimization techniques, of which they had no idea what they did, or what the differences were. They didn't have to worry if the design met timing via an area optimization or a timing optimization. They just pressed go. This is the level of Automation needed for Structural Analysis of RTL designs. The user sets the design, tells the tool what checks they want run, and the tool tells them what failures they have in the design. There are types of analysis where FV is the only tool in the toolbox of Static Analysis products to find the answer. However, requiring the user to become an expert in Formal, understanding assertion-driven analysis, what asserts should be used and where, to learn a new language all to find these complex corner case analysis issues, is the wrong approach to the design of analysis tools.

Blue Pearl's approach, is to focus on the `A' in EDA. We have multiple tools in our tool box to find the issues in RTL designs, including Formal. But we don't expect (or want) the user to create assertions. Assertion driven static analysis leads to undesirable results, primarily in the form of runtime. Too often the user will create an assertion that causes the formal engine to be unable to prove the necessary requirement, sending the engine into what appears to be a never-ending loop, all while providing the user with limited information on how correct their assertions to provide the proper setup for the tool.

My proposal, and what the workshop will present, is the basic premise that the user should simply not care about what methodology the tool is using to analyze the design. Instead, the designer should be focusing on his area of expertise, hardware design. The last thing the EDA community should be doing is creating a new set of experts on how to run a tool.

Structural Analysis using Formal Verification, differs from a Formal Verification tool. However, it's common for EDA vendors to reuse engines in other tools. When done with FV engines for structural analysis, they take one of the more complicated user experiences (Formal Verification) and force it into what should be the easiest flow in EDA (Structural Analysis). The better solution is to start with an easy-to-use Structural Analysis system, and use FV as method to solve one of the checks. Where FV is required, the EDA tool instead, based on the check requested by the user, determines what tool best fits the design of the circuit, and if Formal is the best, then choose the optimal assertions to provide the proof necessary for the check. If an appropriate assertion set can't be found, another tool should be used.

As part of the workshop, we will show examples of the proper design + check to show CDC analysis as well as more traditional Structural Analysis checks that use both Formal Verification as well as other analysis engines.

Speaker: Scott Bloom - Blue Pearl Software, Inc.
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Expo Hours

Monday, February 26: 5:00pm - 7:00pm

Tuesday, February 27: 2:30pm - 6:00pm

Wednesday, February 28: 2:30pm - 6:00pm

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A DVCon reception is a chance for conference attendees to network at the end of the each day. Come and enjoy cocktails and conversations in a casual environment with the DVCon Exhibitors. Mingle from booth to booth while enjoying food and drinks.

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Booth: 805
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Exhibitor Listing

**Cadence Design Systems, Inc.**
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**CircuitSutra Technologies Pvt. Ltd..**
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CircuitSutra is an Electronics System Level (ESL) design IP and services company, headquartered in India, having development centers in Noida and Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C,C++,SystemC, TLM, IP-XACT, UVM-SystemC, SystemC-AMS, Verilog-AMS. Its core competencies include Virtual Prototype (Development, Verification,Deployment), Architecture & Performance modeling, Co-simulation, Co-emulation, HLS, SoC & System verification.

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www.mentor.com

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Metrics (Technologies)

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www.metrics.ca

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Mirabilis Design is the largest supplier of Electronics System-Level modeling IP. VisualSim IP is used for hardware-software partitioning, power measurement, energy management, clock speed selection, cache/memory sizing, bus topology configuration, and software scheduling and task allocation. VisualSim has over 500 IPs including 65 processor/cores/controllers, memories, caches, buses, I/O, DMA, NoC, workload generators, RTOS, networks and other supporting devices.

OneSpin Solutions

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OneSpin Solutions, a leader in formal verification, is creating the industry’s most advanced formal platform, encompassing agile design evaluation, coverage-driven ABV, and automated DV apps. The world’s leading electronics companies partner with us to pursue design perfection in areas where reliability really counts: safety-critical verification, SystemC/C++ HLS code analysis, and FPGA equivalence checking. OneSpin: Making Electronics Reliable

Oski Technology, Inc.

**Booth: 205**

www.oskitechnology.com

Oski Technology is the trusted global leader for Formal Verification methodology and expertise. Oski serves six out of the top seven semiconductor design companies and leaders in consumer electronics, communications, computing, image processing, data storage, research, defense, education, automotive, and medical industries. Oski has assembled the world’s largest dedicated team of experts that draws on hundreds of man-years of collective experience to provide Oski-proven verification sign-off.

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www.prodesign-europe.com

PRO DESIGN has more than 30 years of experience as provider in the E²MS market. The company's products and services include the proFPGA family of ASIC Prototyping and FPGA systems. The proFPGA system is a complete, scalable and modular multi FPGA solution, which fulfills highest needs in the area of FPGA based Prototyping.
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Truechip Solutions Pvt. Ltd.

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Verifyer AB

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