2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2018
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	21%
Standard IC Design	9%
ASIC /SoC Design	34%
DSP Design	4%
Microprocessor/Microcontroller Design	10%
IP Development	16%
Library Development	4%
Analog/Mixed Signal	8%
EDA Methods & Tools	29%
Verification	56%
FPGAs & PLDs	16%
Multi-Chip Modules	4%
PCB Design	4%
Software/Embedded Software	12%
Student	3%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	15%
Engineering Management	16%
Design Engineer	11%
System Architecture	3%
Application Engineer	5%
Marketing	3%
Technical Marketing	3%
Product Marketing	3%
Sales	4%
Research/Academic	2%
CAD	3%
Verification Engineer	29%
Software Engineer	3%
Student	2%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	43%
<1M	6%
1 - 5M	6%
5 - 10M	8%
10M - 50M	9%
50 - 100M	8%
>100M	20%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	48%
VHDL	17%
C/C++	36%
SystemC	17%
SystemVerilog	67%
e	4%
Not Applicable	18%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	55%
OVM	2%
VMM	2%
eRM	0%
SystemC/TLM	4%
Proprietary	9%
Not Involved	46%

FIRST-TIME ATTENDEE

Yes	33%
No	67%