CALL FOR TUTORIALS

DVCON US 2020

March 2 – 5, 2020 • DoubleTree Hotel, San Jose, CA

2020 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL, SystemC and e, as well as general purpose languages such as C, C++, PERL, Tcl, and Python. Tools and methodologies include the use of machine learning, testbench automation, hardware-assisted verification, hardware/software co-verification, formal verification, transaction-level system design, high level synthesis, low power design techniques, 3D chip designs, IP based SoC design methods, reference flows and AMS design.

DVCon is seeking for tutorial topics that are current, have a high-level of interest and offer strong continuing educational content.

Over 285 qualified engineers attended the sponsored tutorials during DVCon 2019. Tutorial sponsors reached a captive audience during the half-day educational sessions and had the opportunity to follow-up with them during breaks, at the exhibits, and following the event.

DVCon is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring either of the Tutorials listed below. Submit proposals by Tuesday, September 24.

Submit Here

DVCON SPONSORED TUTORIAL WITH LUNCHEON: $18,300

Sponsorship Includes:

- Complimentary 8x10 booth on the Exhibit Floor
- Company content specific, individualized Luncheon
- Ability to collect contact information from the Sponsored Luncheon attendees
- Copy of the 2020 Attendee Lists (no email addresses)
- Copy of the Sponsored Tutorial Attendee List (email addresses included)
- Tutorial and Luncheon content will be publicized via monthly newsletters, DVCon website, Conference Program and in the Opening Session presentation slides
- 1 dedicated email distribution to the DVCon mail list
- Other promotional items like banners, flyers, gift items, etc. can be distributed at these two events
- Presenters for the tutorial and lunch are entitled to a complimentary one-day registration
- Up to 10 complimentary one-day registrations for the tutorial and lunch presentation

For more information concerning the conference, please contact the conference management, Nannette Jordan at Nannette@mpassociates.com

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TUTORIAL PROPOSAL REQUIREMENTS

Deadline: September 25, 2019

DVCon tutorials are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the tutorial.

- Attendee expectations are high regarding currency of topic, depth of engineering content and breadth of real-life examples
- The Tutorial Chair will review final presentation materials to ensure high quality educational content
- Include suggested presenters names, affiliations & biographies
- Your proposal should be a short abstract of the tutorial, two to five paragraphs, 1,000 words maximum
- Presentation slides need to be supplied in an electronic format in advance of the conference. Presentation slides will be distributed to the attendees in electronic format. Hard copies will not be provided
- Please indicate if this tutorial is a "hands-on" session or lecture format
- Any necessary additional hardware that you may require must be provided by the tutorial organizers

SUGGESTED TOPICS

- SystemVerilog for Verification and/or Design
- SystemC /C/C++ Design and/or Verification of systems.
- SoC and Software-driven Verification
- Assertion-based Verification. SystemVerilog Assertions, PSL, etc.
- Coverage-driven Verification
- High-level Synthesis
- Low-power Design and Verification techniques
- Secure/Encrypted IP-based SoC design methods
- Debug for design and verification
- Mixed-signal modeling and verification
- Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT)
- Functional Safety
- Security
- Embedded software verification
- Hardware/Software Co-development
- Verification Productivity Methods
- Formal Methodology and Static Analysis
- Emulation
- Post SI Debug
- FPGA Prototyping
- Moving from proprietary solutions to standards-based design and verification
- Portable Stimulus
- Machine Learning driven techniques

TUTORIAL DEADLINES

September 24, 2019: Proposals due. Submit at **DVCon.org**

November 5, 2019: Accept/Reject notification

November 28, 2019: All Tutorial content due for Conference Program and website: tutorial title, abstract, speaker names, affiliations and biographies

January 7, 2020: Draft Presentation slides due to DVCon Tutorial Chair

January 14, 2020: Presentation feedback due to presenters on slides

February 11, 2020: Final slides due for final production for attendee distribution

CONFERENCE SCHEDULE

Monday, March 2
- Accellera Day Tutorials
- Short Workshops
- Exhibits

Tuesday, March 3
- Technical Sessions
- Keynote Speaker
- Exhibits

Wednesday, March 4
- Technical Sessions
- Panel Discussion
- Exhibits

Thursday, March 5
- Tutorials
- Short Workshops

SPONSORED BY: Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. **Accellera.org**

Conference Sponsor:

accellera SYSTEMS INITIATIVE™

General Chair
Aparna Dey- *Cadence Design Systems, Inc.*
aparna@cadence.com

Tutorial Chair
Ambar Sarkar- *NVIDIA Corp.*
ambars@nvidia.com