Tuesday 8:15 AM - 8:45 AM			
Opening Session			
Tuesday 9:00 AM - 10:30 AM			
Session #	**Day**	**Session and Paper Title**	**Room**
	Tuesday	**Formal Verification I**	**OAK**
10.2		Novel Approaches for C vs. RTL Formal Verification of Vertex Attribute Address Generator Unit	
10.3		Formal Verification by the Book: Error Detection and Correction Codes	
1.3		Finding the Last Bug in a CNN DMA Unit	
	Tuesday	**Portable Stimulus**	**FIR**
3.1		Machine Learning-Guided Stimulus Generation for Functional Verification	
2.2		Designing PSS Environment Integration for Maximum Reuse	
10.4		Second Generation Completeness Analysis of Formal Assertions on Compatibility of RISC-V Cores	
Tuesday 10:30 AM - 12:00 PM			
Poster Session			**GATEWAY FOYER**
Tuesday 12:00 PM - 1:15 PM			
Lunch			**PINE/CEDAR**
Tuesday 1:30 PM - 2:30 PM			
Panel	**Tuesday**	**New Chip Designs Create Tidal Wave of Change**	**OAK/FIR**
Tuesday 2:30 PM - 6:00 PM			
Expo	**Bayshore Ballroom**		
Tuesday 3:00 PM - 5:00 PM			
Session #	**Tuesday**	**UVM Strategies**	**OAK**
5.1		UVM – Stop Hitting Your Brother Coding Guidelines	
9.2		UVM Layering for Protocol Modeling Using State Pattern	
5.3		UVM Reactive Stimulus Techniques	
Session #	**Tuesday**	**Verification Potpourri**	**FIR**
6.1		What Your Software Team Would Like the RTL Team to Know	
6.2		It Should Just Work! Tips and Tricks for Creating Flexible, Vendor Agnostic Analog Behavioral Models	
6.3		Rolling the Dice with Random Instructions is the Safe Bet on RISC-V Verification	

6.4		Multi Level Replay of VIP Models in Isolation from Original Design Verification Environment to Enhance Protocol Analysis and Debug	
Session #	**Tuesday**	**Power-Aware Design and Verification**	**MONTEREY/CARMEL**
7.1		UPF 1.0, UPF 2.0, UPF 2.1, UPF 3.0, and Now UPF 3.1: The Big Q "Which is the Right Standard for My Design?"	
7.2		Low-Power Verification at Gate Level for Zen Microprocessor Core	
7.3		May the Powers be With You! – Unleashing Powerful New Features in UPF IEEE 1801	
7.4		Did Power Management Break My CDC Logic? An Integrated Approach to Power Domain and Clock Domain Crossing Verification	
		Wednesday 8:30 AM - 11:30 AM	
	Wednesday	**Tutorial 3: Application Optimized HW/SW Design & Verification of a Machine Learning SoC**	**OAK**
		Wednesday 8:30 AM - 10:00 AM	
	Wednesday	**Short Workshop 9: Mind the Gap(s): Closing and Creating Gaps Between Design and Verification**	**FIR**
		Wednesday 10:15 AM - 11:45 AM	
	Wednesday	**Short Workshop 10: SystemRDL to PSS Basic to Pro**	**FIR**
		Wednesday 12:00 PM - 1:15 PM	
Lunch			**PINE/CEDAR**
		Wednesday 1:30 PM - 2:30 PM	
Industry Talk	**Wednesday**	**FPGA Verification Maturity: A Quantitative Analysis**	**OAK/FIR**
		Wednesday 2:30 PM - 6:00 PM	
Expo	**Bayshore Ballroom**		
		Wednesday 3:00 PM - 4:30 PM	
Session #	**Wednesday**	**Verification Processes and Methodologies**	**OAK**
11.1		The Verification Cockpit - A One-Stop Shop for Your Verification Data	
11.2		Using Static RTL Analysis to Accelerate Satellite FPGA Verification	
11.3		Eradicating X-Bugs and Achieving Higher Design Quality Using Static X-Propagation Sign-Off	

Session #			
	Wednesday	SystemVerilog Solutions	FIR
12.1		SystemVerilog Constraints: Appreciating What You Forgot in Class to Get Better Results	
12.2		SystemVerilog Configurations and Tool Flow Using SCons (An Improved Make)	
12.3		A SystemVerilog Framework for Efficient Randomization of Images With Complex Inter-Pixel Dependencies	

Session #			
	Wednesday	Reset Domain Challenges	MONTEREY/CARMEL
13.1		Systematic Methodology to Solve Reset Challenges in Automotive SoCs	
13.2		Scalable Reset Domain Crossing Verification Using Hierarchical Data Model	
13.3		Innovative Techniques to Solve Complex RDC Challenges	

Wednesday 4:45 PM - 5;00 PM		
Best Paper / Poster Presentation Award		**Bayshore Ballroom**