FEBRUARY 24 - 26, 2009

DOUBLETREE HOTEL

SAN JOSE, CA

WWW.DVCON.ORG

DVCon

design & verification conference & exhibition

Sponsored by:

accellera

Final Program

General Chair's Welcome

Welcome to DVCon '09 everyone!

DVCon is the premier conference for functional design and verification of digital electronic systems. The conference is focused on bringing you information from the leading edge of technology, techniques, standards and methods. We continually strive to enhance the value of DVCon to make it worth the investment of your time in attending, so this year we have extended the technical program to include three additional paper sessions and have expanded the exhibit hours. As always, the program offers sponsored tutorials, vendor-sponsored lunches (and breakfast, too), with plenty of other educational and entertaining features.

Our keynote speaker, Dr. Aart de Geus, will discuss "The Techonomics of Verification," in which he will explore the economic and technological factors driving demand for more comprehensive verification solutions, and the opportunities for solving these challenges. In our efforts to continue evolving the conference, we will be following a new path with the popular "Executive Panel," which will be moderated this year by Peggy Aycinena. Peggy has brought together an impressive array of senior EDA executives to discuss "EDA: Dead or Alive?" which is sure to be a lively discussion on the future of our industry. Don't miss this new perspective on an old DVCon favorite. Last, but not least, we'll be closing the technical program with an in-depth panel discussion on "Mixing Formal Analysis with Simulation."

As our industry grows and evolves, DVCon will grow and evolve with it. As you can see, this year's program continues our tradition of providing a high level of educational and practical material that everyone can use in their daily work life. Our research-oriented papers provide a peek into future innovations and advances in our industry. The successful sponsored tutorial program continues with opportunities for in-depth knowledge of targeted subjects. We have expanded our exhibit floor space to accommodate broader participation from EDA vendors. I hope you will find time to visit our exhibitors to learn first-hand about state-of-the-art solutions.

We endeavor to deliver on the charter of DVCon by improving the functional design and verification of electronic systems. I believe you will find that DVCon 2009 is a great forum for the latest in the design and verification industry.

Tom Fitzpatrick
Mentor Graphics Corp.
2009 General Chair

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Colorado Springs, CO

Conference Sponsor

Accellera

To improve designers' productivity, the electronic design industry needs a methodology based on both worldwide standards and open interfaces. Accellera was formed in 2000 through the unification of Open Verilog International and VHDL International to focus on identifying new standards, development of standards and formats, and to foster the adoption of new methodologies.

Accellera's mission is to drive worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process. Its Board of Directors guides all the operations and activities of the organization, and is comprised of representatives from ASIC manufacturers, systems companies and design tool vendors.

Membership

Accellera's members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, Accellera members have a higher level of visibility in the EDA industry as active participants in Accellera-Sponsored activities and as contributors to its decisions which impact the EDA industry.

www.accellera.org

Technical Committees

The Accellera Board of Directors established the Technical Committee (TC) to develop, update and extend hardware design language (HDL) standards. The TC is comprised of subcommittees that focus on the various standards under development, and report to the TC Chair. In addition, Accellera supports the activities of certain IEEE working groups and cooperates with other standards groups within the EDA industry.

* IEEE P1801 Unified Power Format
* Unified Coverage Interoperability Standard
* Interface Technical Committee
* IEEE P1450.6.1 Open Compression Interface
* Open Verification Libraries
* Verilog AMS
* IEEE P1800 SystemVerilog
* IEEE P1850 PSL
* IEEE P1076 VHDL
* Verification IP

Tuesday, February 24, 2009

7:00am - 6:30pm • Registration (Bayshore Foyer)

Be certain to visit the DVCon Expo for the hottest trends! **2:00 - 6:30pm**

Cocktail Reception (Bayshore Ballroom) **5:00 - 6:30pm**

Tutorial 1 • A Structured Methodology for Verifying Low Power Designs

Sponsored by: SYNOPSYS®

8:30am - 12:00pm (Oak Ballroom)

Tutorial 2 • Applying Proven Verification Strategies that Close Verification Holes

Sponsored by: Mentor Graphics®

8:30am - 12:00pm (Fir Ballroom)

Accellera Luncheon - 12:00 - 1:30pm (Pine/Cedar Ballroom)

Tutorial 3 • OVM in a Multi-language World

Sponsored by: cadence™

1:30 - 5:00pm (Oak Ballroom)

Tutorial 4 • TLM-2.0 in Action: An Example-based Approach to Transaction-level Modeling and the New World of Model Interoperability

Sponsored by: SYSTEMC™

1:30 - 5:00pm (Fir Ballroom)

Tuesday, February 24, 2009

Tutorial Sponsored by: SYNOPSYS®

Room: Oak Ballroom • 8:30am -12:00pm

Tutorial 1 • A Structured Methodology for Verifying Low Power Designs

Organizer: Krishna Balachandran - *Synopsys, Inc.*

Presenters: Janick Bergeron - *Synopsys, Inc.*
Srikanth Jadcherla - *Synopsys, Inc.*
Yoshio Inoue - *Renesas*
John Goodenough - *ARM*

Power Management and Low Power Design bring a whole new assortment of bugs and failure mechanisms to IC designs. The task of verification, already a critical path in the delivery of the chip, now needs to take on additional tests and flows to ensure that the power management scheme is functional.

The complexity of power management and the broad spectrum of design scenarios could easily lead to escaped bugs without a rigorous methodology in place. In this tutorial, we focus first on the complexities and changes brought about in the low power era and the bugs engendered by low power design. We then cover the process of rigorous verification for low power - the setup of testbenches, establishment of testplans, directed and random testing and the metrics of verification using coverage and assertions. We also discuss the process of formal and static verification at various stages in the design flow, including Post layout netlists.

Attendees will be provided with a copy of the book Verification Methodology Manual for Low Power, authored by the presenters.

Tuesday, February 24, 2009

Tutorial Sponsored by: Mentor Graphics®

Room: Fir Ballroom • 8:30am -12:00pm

Tutorial 2 • Applying Proven Verification Strategies that Close Verification Holes

Organizer: Rebecca Granquist - *Mentor Graphics Corp.*
Presenter: Tom Fitzpatrick - *Mentor Graphics Corp.*

This in-depth, half-day verification tutorial shows how to use proven verification methodologies and technologies to close your verification holes. This tutorial shows a detailed strategy for utilizing the modular nature of the Open Verification Methodology (OVM) as the foundation to connect tools like algorithmic testbenches, multi-core software verification engines, verification IP, verification management and others in a comprehensive reusable verification infrastructure.

The race toward successful product releases continues, and the competition is relentless. The electronics industries demand continue to reveal verification holes and EDA suppliers continually invest in new methods and solutions to fill the new rips in the design verification fabric. The progress towards solutions at times appears glacially slow, but contrary to the glacial view, there are demonstrated verification strategies and products that do cover verification holes.

The tutorial begins with an overview of common and very real world verification challenges that project teams have recently encountered and addressed when dealing with verification emergencies. Attendees will be walked through the process of identifying a broad set of technical solutions and be shown detailed examples of how to best integrate them in a comprehensive verification environment. The goal of this tutorial is to give you clarity in today's solutions and working knowledge of how to close your verification holes with a roadmap to utilize them.

The tutorial's detailed technical information of the solutions and OVM interconnect are targeted at design and verification engineers, but managers would also benefit by reviewing the solutions that have provided time to market, i.e. engineering productivity and verification process visibility.

Tuesday, February 24, 2009

Tutorial Sponsored by: cadence™

Room: Oak Ballroom • 1:30 - 5:00pm

Tutorial 3 • OVM in a Multi-language World

Organizer: Adam Sherer - *Cadence Design Systems, Inc.*
Presenters: Umer Yousafzai - *Cadence Design Systems, Inc.*
Brett Lammers - *Cadence Design Systems, Inc.*
Jonathan Bromley - *Doulos Ltd.*

Verification methodologies all have their benefits; but only the Open Verification Methodology (OVM) has the dual advantages of being able to scale to the system-level and across projects while being completely open and interoperable with the majority of the commercial simulation platforms on the market. The OVM can accelerate your verification environment development and integration by providing guidelines and proven building blocks for creating advanced multi-language verification environments, including the ability to leverage multi-language VIP reuse. OVM offers an easy path to get started and leverages a robust class library that encapsulates object-oriented and aspect-oriented capabilities for building coverage-driven environments.

This tutorial will showcase the many advantages of OVM multi-language verification to maximize ROI and enable your design and verification teams to use their preferred verification language.

Don't miss this chance to hear more about the OVM in this tutorial that includes presentations, demonstrations, and a panel of users and industry experts taking a deeper look at how the OVM plays a key role in their verification process.

Tuesday, February 24, 2009

Tutorial Sponsored by: SYSTEMC™

Room: Fir Ballroom • 1:30 - 5:00pm

Tutorial 4 • TLM-2.0 in Action: An Example-based Approach to Transaction-level Modeling and the New World of Model Interoperability

Organizers: Jack Donovan - *XtremeEDA Corp.*
Jill Jacobs - *Mod Marketing*
Presenters: David C. Black - *XtremeEDA Corp.*
John Aynsley - *Doulos Ltd.*
Zhu Zhou - *Intel Corp.*
Frank Schirrmeister - *Synopsys, Inc.*

Transaction-level modeling (TLM) continues to grow in importance for architectural exploration, performance analysis, building virtual platforms for software development, and functional verification. The TLM interface standard enables SystemC model interoperability and reuse at the transaction level, providing an essential framework for system-level design. The June 2008 adoption of TLM-2.0 as an OSCI standard marks the culmination of several years of intensive work. Significant effort has been invested in developing examples to describe and demonstrate the draft standard's content.

This tutorial will present the details of TLM-2.0 using an examples-based approach and how to get the most value out of using the standard. The examples demonstrate the modeling styles, as well as integration of legacy models based on TLM-1 interfaces, which are fully preserved in TLM-2.0.

Highlights Include:

1. An overview of the concepts and the intent of the TLM-2.0 standard including a brief history of transaction level modeling in SystemC and the next steps for TLM-2.0.
2. An Introduction to TLM 2.0 concepts.
3. A brief introduction to the TLM 2.0 LRM, plans for the LRM, and some fine points of the standard that have emerged during the LRM development process.
4. An introduction to the TLM 2.0 examples.
5. An example of TLM 2.0 concepts for a real life component.
6. An example of application of TLM 2.0 concepts to a system design.

Tuesday, February 24, 2009

Room: Pine/Cedar Ballroom • 12:00 - 1:30pm

Accellera Luncheon ◦ Accellera Technical Committee Update

Organizers: Lynn Horobin, David Lin - *Accellera Organization, Inc.*
Presenters: Shrenik Mehta - *Accellera Chairman, Sun Microsystems, Inc.*
Karen Pieper - *Accellera Technical Committee Chair, Tabula, Inc.*

Accellera, sponsor of the Design & Verification Conference, is a leading-edge EDA standards organization that provides design and verification standards for quick availability and use in the electronics industry. Conference attendees are invited to join us for a complimentary luncheon and watch a presentation on current standards activities featuring the exciting progress of the recently-formed committee to define a standard verification IP methodology.

Wednesday, February 25, 2009

Room: Pine/Cedar Ballroom • 7:00 - 8:15am

Breakfast ◦ Prototyping: Where Hardware and Software First Meet

Organizer: Nancy Weiss - *Synopsys, Inc.*
Speaker: Ken McElvain - *Synopsys, Inc.*

Sponsored by: SYNOPSYS®

With the increase of software content in SOCs, completion of software development and its verification are becoming the biggest expense and critical path to product release. This creates an intense pressure to begin productive software development and verification prior to silicon availability. Ken will review the different pre-silicon prototypes that have emerged to support early software development with virtual platforms and hardware prototypes. The SOC software development tasks will be outlined with a focus on how the prototypes produced by the hardware team can be enhanced to improve software development productivity and also generate valuable information to validate architecture decisions.

Wednesday, February 25, 2009

7:30am - 6:30pm • **Registration** (Bayshore Foyer)

DVCon Expo — ***Last opportunity to visit the DVCon Expo for the hottest trends!*** **1:00 - 6:30pm**

Cocktail Reception (Bayshore Ballroom) **5:00 - 6:30pm**

7:00 **Breakfast : Prototyping: Where Hardware and Software First Meet** Sponsored SYNOPSYS (Pine/Cedar Ballroom)

8:15 **Opening Session** (Oak Ballroom)

	Fir Ballroom	Oak Ballroom
9:00 10:30	**Session 1** Verification Methodology and Testbenches - I	**Session 2** Formal Verification Applications
	Break	
11:00 12:30	**Session 3** Increasing Functional Coverage	**Session 4** Emulation/Acceleration

Luncheon: Case Studies of OVM in Multi-language Verification Environment
Sponsored by: cadence (Pine/Cedar Ballroom)

2:00 **Keynote** (Oak/Fir Ballroom)
The Techonomics of Verification
Aart de Geus - *Chief Executive Officer and Chairman of the Board, Synopsys, Inc.*
2:45

Break

3:15 **Panel: EDA: Dead or Alive?**
(Oak/Fir Ballroom)
5:00

Thursday, February 26, 2009

7:30am - 4:00pm • **Registration** (Bayshore Foyer)

Donner Ballroom	Cascade Ballroom	Siskiyou Ballroom	
Session 5 Verification Methodology and Testbenches - II	**Session 6** Low Power Verification	**Session 7** Verification Data Management	8:30 10:00
Break			
Session 8 Verification Methodology and Testbenches - III	**Session 9** Mixed-signal Design and Verification	**Session 10** Case Studies - I	10:30 12:00

Luncheon: Risky Business: How Do I Manage Risk in My Next Design Project?
Sponsored by: Mentor Graphics (Pine/Cedar Ballroom)

Session 11 Low Power Management	**Session 12** Programming with SystemVerilog	**Session 13** Case Studies - II	1:30 3:00
Break			
Panel: Mixing Formal Analysis with Simulation: Why, When, Where, and How? (Donner/Siskiyou Ballroom)			3:30 5:00
Closing Session 2009 Best Paper Award Presentation (Donner/Siskiyou Ballroom)			5:30 6:00

Wednesday, February 25, 2009

Opening Session ◦ 8:15 - 8:45am ◦ Oak Ballroom

Session 1 ◦ Verification Methodology and Testbenches - I

Room: Fir Ballroom • 9:00 - 10:30am

Session Chair: Clifford E. Cummings - *Sunburst Design, Inc.*

1.1 Model-based Instruction Stream Generation for Processor Verification
Van Le, Hans van der Schoot, Michael Warner - *Mentor Graphics Corp.*

1.2 Divide and Conquer: Techniques for Creating Highly Reusable Stimulus Generation Process
Ning Guo - *Paradigm Works, Inc.*

1.3 Attacking Constraint Complexity in Verification IP Reuse
Ben Chen, Harish Krishnamoorthy, Srinath Atluri - *Cisco Systems, Inc.*
Alexander Wakefield, Balamurugan Veluchamy - *Synopsys, Inc.*

Session 2 ◦ Formal Verification Applications

Room: Oak Ballroom • 9:00 - 10:30am

Session Chair: Kenneth Chang - *Cadence Design Systems, Inc.*

2.1 Post-silicon Debug using Formal Verification Waypoints
C. Richard Ho, Michael Theobald, Brannon Batson, J.P. Grossman, Stanley C. Wang, Joseph Gagliardo, Martin M. Deneroff, Ron O. Dror - *D. E. Shaw Research*
David E. Shaw - *D. E. Shaw Research and Columbia Univ.*

2.2 A Novel Application of Formal Analysis to Verify LBIST
Syed Obaidulla, Samir Shah - *Advanced Micro Devices, Inc.*
Darrow Chu - *Cadence Design Systems, Inc.*

2.3 Beyond Assertions: Visualize Protocol Specifications using Assertions with a Formal Property Checker
Thomas J. Thatcher - *Sun Microsystems, Inc.*
Xiaolin Chen - *Synopsys, Inc.*

Wednesday, February 25, 2009

Session 3 ◦ Increasing Functional Coverage

Room: Fir Ballroom • 11:00am - 12:30pm

Session Chair: David Rich - *Mentor Graphics Corp.*

3.1 Improving Simulation Coverage of Metastability Effects in Clock Domain Crossing Verification
Hiroaki Iwashita - *Fujitsu Labs, Ltd.*

3.2 Pull Back the Covers with Embedded Coverage
Stacey Secatch, Russ Nelson, Carl Rohrer - *Xilinx, Inc.*

3.3 Domain Oriented Training for Data Mining Coverage Driven Verification
Edgar Leonardo Romero Tobar, Carlos Ivan Castro Marquez, Marius Strum, Wang Jiang Chau - *Univ. of Sao Paulo*

Session 4 ◦ Emulation/Acceleration

Room: Oak Ballroom • 11:00am - 12:30pm

Session Chair: Jack Donovan - *XtremeEDA Corp.*

4.1 Using Compile-time and Run-time Checks to Overcome the Barriers to Verilog Simulation Acceleration
Jim Foley - *Liga Systems, Inc.*

4.2 An Acceleratable OVM Methodology Based on SCE-MI 2.0
Anoop Saha, Suresh Krishnamurthy, Amit Jain, Sanjay Gupta, Vipul Kulshretha - *Mentor Graphics Corp. (India) Pvt. Ltd.*

4.3 Towards Emulation-based System-level Verification Environments - An Industrial Approach
Alex Goryachev, Shady Copty - *IBM Haifa Research Labs*

Wednesday, February 25, 2009

Room: Pine/Cedar Ballroom • 12:30 - 1:45pm

Luncheon ◦ Case Studies of OVM in Multi-language Verification Environments

Organizer: Adam Sherer - *Cadence Design Systems, Inc.*

Speaker: Mike Stellfox - *Cadence Design Systems, Inc.*

Sponsored by: cadence

Multi-language verification is a reality in most projects today. Driven by legacy, distributed teams, multiple abstraction levels, and/or commercial VIP, verification leaders are innovating solutions to tap the cost savings associated with reuse while managing the complexity of multi-language integration. Several case studies of single and multi-language verification environments will be presented during the luncheon in an interactive design-review format.

Luncheon attendees will be encouraged to ask questions and the presenters will be available to continue the discussions in on-line forums if the interest extends beyond the luncheon time period.

Wednesday, February 25, 2009

Room: Oak/Fir Ballroom • 2:00 - 2:45pm

Keynote Address:

The Techonomics of Verification

Aart de Geus - Chief Executive Officer and Chairman of the Board, *Synopsys, Inc.*

Demand for smaller and more feature-filled devices is driving the semiconductor industry and EDA to innovate new solutions for hardware and software verification. Today's verification challenges are more complex and intertwined than at any other time in the history of Moore's Law, driving verification costs to record levels and magnifying the consequences of verification failure.

The increased visibility and impact of verification across all SoC stakeholders from senior business executives to the system architect, digital designer, custom designer and software developer has driven demand for more comprehensive, holistic approaches to verification. Dr. Aart de Geus will explore the economic and technological factors creating these verification challenges and the opportunities for building a more efficient solution that simultaneously addresses verification requirements from software to silicon.

Bio: Since co-founding Synopsys in 1986, Dr. Aart de Geus has expanded Synopsys from a start-up synthesis company to a world leader in electronic design automation. He is an IEEE Fellow, the recipient of the 2001 Society Industrial Pioneer Award, the 2007 IEEE Robert N. Noyce Medal, the 2007 Silicon Valley Leadership Group (SVLG) "Spirit of the Valley" Lifetime Achievement Award, and the 2008 Phil Kaufman Award. He is also active in the business community as a member of the board of Applied Materials, SVLG, TechNet, the Global Semiconductor Association, and the Electronic Design Automation Consortium.

Wednesday, February 25, 2009

Room: Oak/Fir Ballroom • 3:15 - 5:00pm

Panel ◦ EDA: Dead or Alive?

Moderator: Peggy Aycinena - *Editor, EDA Confidential*

The EDA industry is suffering from a severe case of schizophrenia. One half of the EDA Brain Trust says the industry is Brain Dead, the other half says there's nothing but Good Times ahead. Can we actually have it both ways? Is the industry stuck in the past with legacy tools, customers, and mindsets – or is there really an exhilarating future ahead? Ten years from now, will a re-energized EDA industry be generating billions and billions of dollars with third-party tools for cutting-edge technologies and expanded markets? Or, will there even be an EDA industry ten long years from now?

Please join us as we try to predict the future, in light of hits and misses from the past.

Questions for the panelists will come from the emerging EDA Blogosphere, and will cover everything from soup to nuts as we try to decide if EDALive! is more illusion or reality.

Panelists: Ajoy Bose - *Chairman President & CEO, Atrenta, Inc.*
Diana Feng Raggett - *CEO, President & Co-Founder of Javelin Design Automation, Inc.*
Gary Meyers - *VP & GM of Synplicity Business Group, Synopsys, Inc.*
Lauro Rizzatti - *GM, EVE-USA*
Ravi Subramanian - *CEO, Berkeley Design Automation, Inc.*
Scott Sandler - *President, SpringSoft, Inc.*
Tom Sandoval - *CEO, Calypto Design Systems*

Presentation of the Technical Excellence Award

Accellera's Technical Excellence Award recognizes the outstanding achievements of its Technical Subcommittee members in creating electronic design standards. The winner of 2009 Technical Excellence Award will be publicly recognized at DVCon.

Thursday, February 26, 2009

Session 5 ◦ Verification Methodology and Testbenches - II

Room: Donner Ballroom • 8:30 - 10:00am

Session Chair: Ambar Sarkar - *Paradigm Works, Inc.*

5.1 Adding New Dimensions to Verification IP Reuse
Gaurav-Kumar Verma, Rudra Mukherjee - *Mentor Graphics Corp.*

5.2 Unified Formal and Dynamic Verification Closure: Can Mutations Bridge the Gap?
Olivier Haller, Mickael Moreau, Laurent Martin-Borret, Sofiene Mejri, Mirella Negro Marcigaglia - *STMicroelectronics*

5.3 Adopting a Methodology and Flow for Reuse and Quality of Verification
Dinesh Kumar Malviya - *Rambus Chip Tech. (India) Pvt. Ltd.*

Session 6 ◦ Low Power Verification

Room: Cascade Ballroom • 8:30 - 10:00am

Session Chair: Greg Tumbush - *Tumbush Enterprises, LLC*

6.1 Combining Verification Methods for SoC Low Power Verification
Gabriel Duffy, Thomas Goust, Bernard Ramanadin - *ST-NXP Wireless*

6.2 Check Power State Transitions: Can They Impact Critical Transactions?
Paparao S. Kavalipati, Andrew Seawright - *Mentor Graphics Corp.*

6.3 Verification of Low Power Designs with Static, Dynamic, and Formal Methods
Will Chen, Dan Benua, Godwin Maben - *Synopsys, Inc.*

Thursday, February 26, 2009

Session 7 ◦ Verification Data Management

Room: Siskiyou Ballroom • 8:30 - 10:00am

Session Chair: Harry Foster - *Mentor Graphics Corp.*

7.1 Harvesting Real Productivity from Simulation Farms
Matthew Ballance - *Mentor Graphics Corp.*

7.2 SoC Regression Organization and Optimal Job Management
Ynon Cohen - *Cadence Design Systems, Inc.*

7.3 Sample-path Coverage: Stochastic Model Application for Random Testing
Victor Besyakov - *Tundra Semiconductor Corp.*

Session 8 ◦ Verification Methodology and Testbenches - III

Room: Donner Ballroom • 10:30am - 12:00pm

Session Chair: Paul Marriott - *XtremeEDA Corp.*

8.1 Guidelines for Writing Formal, Friendly Assertions
Manoj Kumar Thottasseri, **Mandar Munishwar** - *Synopsys, Inc.*
Gaurav Gupta - *Synopsys, Inc. (India) Pvt. Ltd.*

8.2 Using Parameterized Classes and Factories - The Yin and Yang of Object-oriented Verification
David Rich, Adam Erickson - *Mentor Graphics Corp.*

8.3 Improving Efficiency and Productivity While Improving Coverage using SystemVerilog OVM Registers
Mogens Lyngsie - *Nokia*
Rich Edelman, Allan Crone, Mark Peryer, Raghu Ardeishar- *Mentor Graphics Corp.*

Thursday, February 26, 2009

Session 9 ◦ Mixed-signal Design and Verification

Room: Cascade Ballroom • 10:30am - 12:00pm

Session Chair: Thomas J. Sheffler - *Consultant*

9.1 Validating WiMAX OFDMA using SystemVerilog and VMM
Albert Chiang, Wei-Hua Han - *Synopsys, Inc*
Bhanu Kapoor - *Mimasic*

9.2 A SystemVerilog Approach for Analog/Mixed-signal Verification
Shyam Rapaka, Tapan Halder - *Synopsys, Inc.*
Vikas Chandra - *ARM*

9.3 Get to ASICs Faster - A Novel Mixed-signal Design Methodology
Greg Tumbush - *Tumbush Enterprises, LLC*
Gareth Weale, Dustin Griesdorf, William Gonnason, Marc Matthey, Andreas Drollinger, Alaa El-Agha - *ON Semiconductor*
Holger Meiners - *Consultant*

Session 10 ◦ Case Studies - I

Room: Siskiyou Ballroom • 10:30am - 12:00pm

Session Chair: Stan Krolikoski - *Cadence Design Systems, Inc.*

10.1 Verification Case Studies: Evolution from SVA 2005 to SVA 2009
Dmitry Korchemny, Erik Seligman - *Intel Corp.*
Surrendra Dudani, Eduard Cerny - *Synopsys, Inc.*
Lisa Piper - *Consultant*

10.2 Cost Evaluation for Adopting Formal Property Checking: a Detailed Case Study
Richard Boulton - *Icera, Inc.*
Mark Handover - *Mentor Graphics Corp. UK Ltd.*

10.3 Adding Last-minute Assertions to a Design and Verification Project: Lessons Learned (a little late) about Designing for Verification
Stuart Sutherland - *Sutherland HDL, Inc.*

Thursday, February 26, 2009

Room: Pine/Cedar Ballroom • 12:00 - 1:15pm

Luncheon ◦ Risky Business: How Do I Manage Risk in My Next Design Project?

Organizer: Stephen Bailey - *Mentor Graphics Corp.*

Sponsored by Mentor Graphics

Designing electronic systems is difficult and shouldn't be left to the Joel Goodsons of the world (Tom Cruise's character from Risky Business). Challenges and risks abound through-out the life of every electronic system design project. Successful projects depend on the ability to manage risk and minimize factors that can cause schedule delays or worse. The need to more effectively manage projects has led to increased interest and reliance on verification management systems.

Come join Mentor Graphics for a sometimes irreverent, sometimes entertaining and always informative discussion on managing risk by managing verification.

YOU BE THE JUDGE!

Best Paper Award

Conference Attendees Vote for the Best Paper for 2009

Recognition of quality paper contributions to the technical program this year will be decided by choosing the best paper of the conference. The voting will be on a scale of 1 to 7, with 7 being for great, high quality papers and 1 for papers you may not have gleaned as much value from. Your vote can be based on attending the session or reading the paper from the proceedings. Please do not vote for a paper that you have no opinion on.

Votes are due Thursday, February 26 by 3:00pm.
Please return the forms to the registration desk.

Presentation – Thursday, February 26 at 5:00pm at the closing session in the Donner Ballroom.

Thursday, February 26, 2009

Session 11 ◦ Low Power Management

Room: Donner Ballroom • 1:30 - 3:00pm

Session Chair: Dan Benua - *Synopsys, Inc.*

11.1 OVM Based Methodology for Low Power Designs
Neyaz Khan, John Decker - *Cadence Design Systems, Inc.*

11.2 ESL Specification, Generation, and Visualization using IEEE-1801 Power-managed SoCs (PM-SoCs)
J. Marc Edwards, John Swanson - *Synopsys, Inc.*
Gary Delp - *LSI Corp.*
Rami Rachamim - *Mentor Graphics Corp.*

11.3 Low Power Verification Methodology using UPF
Freddy Bembaron- *Texas Instruments, Inc.*
Rudra Mukherjee, Amit Srivastava, Sachin Kakkar - *Mentor Graphics Corp.*

Session 12 ◦ Programming with SystemVerilog

Room: Cascade Ballroom • 1:30 - 3:00pm

Session Chair: Ning Guo - *Paradigm Works, Inc.*

12.1 Towards an Object-oriented Design Methodology using SystemVerilog
Sachin Kakkar, **Rudra Mukherjee** - *Mentor Graphics Corp.*

12.2 VPI for SystemVerilog Goes Dynamic
John J. Shields, Abigail Moorhouse - *Mentor Graphics Corp.*
Ying-Tsai Chang - *SpringSoft, Inc.*

12.3 Is There a Future for SystemVerilog Interfaces?
Jonathan Bromley - *Doulos Ltd.*
Gordon Vreugdenhil - *Mentor Graphics Corp.*

Thursday, February 26, 2009

Session 13 ◦ Case Studies - II

Room: Siskiyou Ballroom • 1:30 - 3:00pm

Session Chair: Shankar Hemmady - *Synopsys, Inc.*

13.1 Building a Reusable SV CRV Environment for Verifying Multiple Versions of a SATA Sub-system
Minh Le - *Texas Instruments, Inc.*
Rahul Malvi, Archana Rai - *Qthink, Inc.*

13.2 Adapting Legacy Verification Models for Use in VMM
Michael Blake - *Ericsson*
Chris Spear - *Synopsys, Inc.*

13.3 Achieving Verification Goals for External IP - Is Buying 3rd Party VIP Sufficient?
Leena Singh, Faisal Haque - *Qualcomm, Inc.*

SEE YOU NEXT YEAR!

MARK YOUR CALENDAR

DVCon design & verification conference & exhibition

FEBRUARY 23-25, 2010!

Thursday, February 26, 2009

Room: Donner/Siskiyou Ballroom • 3:30 - 5:00pm

Panel ◦ Mixing Formal Analysis with Simulation: Why, When, Where, and How?

Organizer: Tom Anderson - *Cadence Design Systems, Inc.*
Moderator: Mike Stellfox - *Cadence Design Systems, Inc.*

Formal verification has long been viewed as complementary to simulation-based verification, able to solve certain problems much better. This begs the question of how they should complement each other. Customers are experiencing varying degrees of success, yet there isn't an industry accepted approach. What are the factors to consider when determining the balance? How are teams coordinated and regressions organized? How are projects monitored and controlled? What are the caveats and risks? How is the information from simulation and formal analysis combined for unified viewing and storage? How much control and methodology should be left to the users to mix formal analysis and simulation? How much integration technology is important when combining them? How is advanced methodology deployed to the mainstream users and projects? What are the problems that persist today with adoption of formal analysis in a simulation methodology such as the OVM or VMM? What areas should EDA companies invest in to further leverage the benefits of combined formal and simulation methodology and technology?

Panelists: Thomas J. Thatcher - *Sun Microsystems, Inc.*
Olivier Haller - *STMicroelectronics*
Yirng-An Chen - *Marvell Technology Group Ltd.*
Lawrence Loh - *Jasper Design Automation, Inc.*
Dan Benua - *Synopsys, Inc.*
Harry Foster- *Mentor Graphics Corp.*
Axel Scherer - *Cadence Design Systems, Inc.*

The DVCon Expo 2009 consists of vendors displaying the latest in Hardware Description Languages, Hardware Verification Languages and EDA tools for the design and verification of electronic systems and integrated circuits.

Exhibiting Companies (as of 01.23.09)

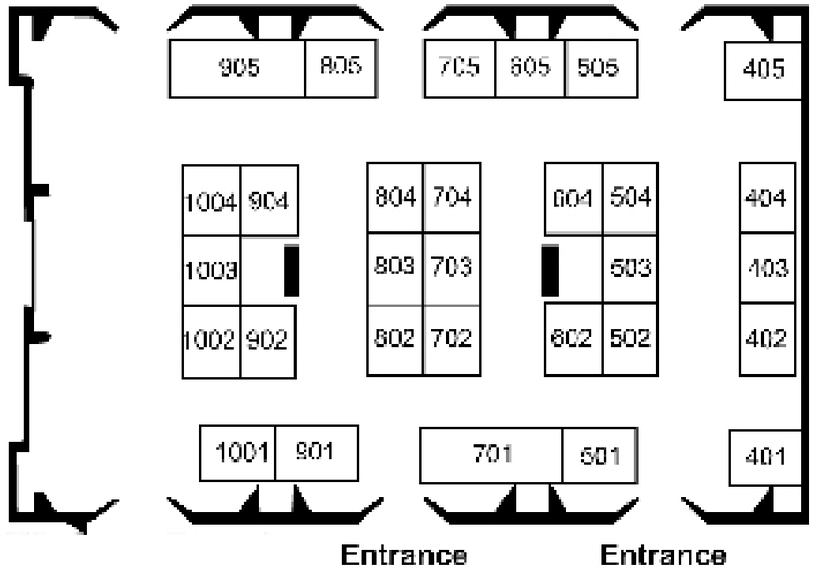
Achilles Test Systems	1002
Aldec, Inc.	605
Averant, Inc.	604
Breker Verification Systems	704
Cadence Design Systems, Inc.	405
Certess	805
Consultants' Corner Innovative Logic Inc.	503
Denali Software, Inc.	904
Dini Group	705
Doulos Inc.	501
eInfochips	804
EMA Design Automation	504
EVE-USA	402
GateRocket, Inc.	505
Jasper Design Automation	902
Mentor Graphics Corp.	701
nSys Design Systems Pvt. Ltd.	702
OneSpin Solutions	502
Open SystemC Initiative (OSCI)	901
Paradigm Works, Inc.	1004
QThink, Inc.	602
Real Intent, Inc.	403
SpringSoft Inc.	1001
Synopsys, Inc.	905
Veritools, Inc.	404
Zocalo Tech, Inc.	401

Expo Hours

Tuesday, February 24, 2009	**2:00 - 6:30pm**
Wednesday, February 25, 2009	**1:00 - 6:30pm**

in the Bayshore Ballroom

Bayshore Ballroom



Achilles Test Systems

Booth # 1002
18 Cedarcroft Lane
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781-330-3738
www.achillestest.com

Achilles Test Systems products and services enable verification teams to correlate test results across multiple project data files, cutting debug time in a collaborative development process. Project status is always available and up to date with automatically generated tables and charts to highlight trends from historical data. Every member of a global team just needs a web browser to contribute insights and to access an integrated visualization of seed tracking, test data, and source code revision history.

Aldec, Inc.

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702-990-4400
www.aldec.com

Aldec Inc., a leader in electronic design verification, offers a patented technology suite including: design creation, HDL simulators, design rule checking, hardware-assisted verification, DO-254 compliance tool set, DSP co-simulation and engineering specialty solutions. Aldec tools handle: VHDL, Verilog®, SystemVerilog, SystemC, Assertions, debugging, code coverage and linting. Aldec is "The Best Value in EDA" providing 25 years of verification. Aldec is a privately held and employs approximately 200 people worldwide. Product demonstrations are located in the DVCon exhibit area Booth #605.

Averant, Inc.

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510-581-8881
www.averant.com

Averant provides Solidify, the premier property verification tool available in the market today. Solidify takes designs written in Verilog, VHDL or mixed-language and properties in SVA, PSL, OVL and HPL (Averant's expressive and easy to use property language), and verifies the properties hold of the design. Solidify also contains a set of automatic checks for common issues such as deadlock and deadcode, a static coverage analysis tool for measuring the completeness of the properties, a testbench-free bug hunting technology for uncovering deep bugs, and a protocol verification tool codeveloped with ARM (called SolidPC) for verifying AMBA TM protocols.

Breker Verification Systems

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8217 Edgemoor Pl.
Austin, TX 78749
512-289-7788
www.brekersystems.com

Breker's Trek™ Graph-Based Test Program Generation technology provides functional verification engineers with an automated solution for generating input stimulus, checking output results and measuring scenario coverage.

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Cadence Design Systems, Inc.

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www.cadence.com

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence® software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

Certess

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Campbell, CA 95008
408-370-6411
www.certess.com

Certess, Inc. is the provider of functional qualification tools for systems-on-a-chip (SoCs) and intellectual property (IP) blocks. The company's flagship product, Certitude, provides verification engineers with an objective way to evaluate and improve the completeness of the verification environment, resulting in shorter and more predictable process to integrate SoC designs. Certitude easily complements all existing verification environments. Certess' customers include the largest system integrators and semiconductor suppliers.

If there was a bug in your design, could you find it?

Consultants' Corner

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Santa Clara, CA 95054
408-200-7443
www.inno-logic.com

Innovative Logic is the leading provider of reusable standard based IP solutions as well as high quality and reliable design services in ASIC, FPGA, and Embedded Systems Design. Innovative Logic has a world class team of engineers who have successfully executed different projects using the latest tools and the technologies. Innovative Logic is headquartered in Santa Clara, CA and has state of art Design Center in Santa Clara, CA and Bangalore, India. For details, please visit our website at www.inno-logic.com.

Denali Software, Inc.

Booth # 904
1000 Hamlin Ct.
Sunnyvale, CA 94089
408-743-4200
www.denali.com

Denali Software, Inc., is a world-leading provider of electronic design automation (EDA) software and intellectual property (IP) for system-on-chip (SoC) design and verification. Denali delivers the industry's most trusted solutions for deploying PCI Express, NAND Flash and DDR DRAM subsystems. Developers use Denali's EDA, IP and services to reduce risk and speed time-to-market for electronic system and chip design. More information about Denali, its products and services is available at www.denali.com.

Dini Group

Booth # 705
7469 Draper Ave.
La Jolla, CA 92037
858-454-3419
www.dinigroup.com

The Dini Group will display the new DN7020K10 with 50 million+ ASIC gates. This logic emulation platform holds 20 of the largest Altera Stratix III FPGAs. This board is the largest and fastest ASIC prototyping engine in production. Other products include powerful PCI, PCI-X, PCIe, and USB hosted FPGA boards based on Xilinx Virtex-5 and Altera StratixII/StratixIIGX. The Dini Group, founded in 1995, has supplied over 5 billion ASIC gates they have driven prices below 1/4 Cent/ASIC gate.

Doulos Inc.

Booth # 501
16165 Monterey Rd.
Morgan Hill, CA 95020
408-776-1370
www.doulos.com

Doulos is the global leader for the development and delivery of world class training solutions for SoC, FPGA and ASIC design and verification. Fully independent, Doulos sets the industry standard for high quality training including SystemVerilog, Verilog®, VHDL, SystemCTM , and ARM-based design.

Since 1991, Doulos has contributed to the success of more than 700 companies across 35 countries. The natural partner for leading tool and technology companies, Doulos schedules classes across the U.S and delivers in-house training world-wide.

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408-496-1882
www.enfochips.com

eInfochips, based in Sunnyvale CA, is a leading provider of IP leveraged silicon design and verification and product design services. Our capabilities extend from spec-silicon-system, with expertise spanning front-end design, ASIC/SoC verification, automated verification methodologies using HVLs, physical layout & implementation, system validation, ASIC prototyping, board design and industry-standard IP development. eInfochips' offshore design centers have delivered multitude silicon and product design solutions to technology companies worldwide, helping customers reduce their time to market and build market strength.

EMA Design Automation

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Rochester, NY 14623
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www.ema-eda.com

EMA Design Automation offers a full line of EDA products to meet all of your IC and PCB design needs. Featuring products from Cadence® Design Systems, EMA offers Cadence Virtuoso® custom design platform, Cadence Incisive® functional verification platform, Cadence Encounter® Conformal® Equivalence Checker, Cadence design-for-manufacturing (DFM) solutions, Cadence PSpice® analog simulation, and Cadence Allegro® and OrCAD® PCB design technologies. EMA also provides TimingDesigner® for advanced digital timing analysis. Visit EMA Design Automation in booth 305.

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Jasper Design Automation is a privately-held EDA software company leveraging formal technologies to deliver high value solutions for the design and verification of electronic systems and semiconductors. The company delivers products utilizing advanced formal analysis and Behavioral Indexing™ technologies to the global electronics market. At DVCon, Jasper will demonstrate recently-announced ActiveDesign, and unveil another innovative design solution. Headquartered in Mountain View, California, Jasper has offices and distributors in North America, South America, Europe, and Japan. Visit Jasper online at http://jasper-da.com.

Tuesday and Wednesday
Receptions at 5:00pm
Bayshore Ballroom
All are welcome!

Mentor Graphics Corp.

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Whether it's called a spark of creativity, a moment of brilliance or a profound idea, the goal of innovation is to create positive change. At Mentor Graphics® our innovative approach to solving customer problems is what makes our functional verification technology so unique. Technology that is not bound by the status quo, but instead reaches to new heights to bring increased productivity to the customers we serve. Come see us at booth #701 and discover how we can work together.

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Open SystemC Initiative (OSCI)

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www.systemc.org

OSCI is dedicated to advancing SystemC™ as an open standard for system-level modeling, design and verification. Leading companies use SystemC for architectural exploration and to deliver high-performance interoperable models of their hardware blocks at various abstraction levels. OSCI recently announced the transaction-level modeling standard, TLM-2.0. The standard provides an essential framework for ESL design and IP reuse. OSCI also released a whitepaper introducing design and modeling of embedded Analog/Mixed-signal systems using SystemC extensions. The TLM kit and whitepaper are available under open source license at www.systemc.org.

Paradigm Works, Inc.

Booth # 1004
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Andover, MA 01810
978-824-1400
www.paradigm-works.com

Paradigm Works is a leading chip development services and software company recognized for engineering excellence, integrity in business, and overall productivity and cost effectiveness. We offer verification services in all of the leading languages, including SystemVerilog, 'e', SystemC, Vera.
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QThink offers flexible technical and business engagement models offering design services ranging from architecture, specification, to logic design and verification, to physical implementation. We are committed to excellence, leveraging QThink engineers with extensive knowledge of RTL design and verification techniques who employ robust and optimized methodology to consistently demonstrate on-time and right-by-construction deliverables. QThink utilizes the latest design automation platforms from the leading EDA suppliers. QThink's centers of excellence are located in San-Diego and San Jose, California and Bangalore India.

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www.realintent.com

Real Intent is extending breakthrough formal technology to critical problems encountered by design and verification teams worldwide. Real Intent's products dramatically improve the functional verification efficiency of leading edge application specific integrated circuit (ASIC), system-on-chip (SOC), and Field Programmable Gate Array (FPGA) devices. This unique application of formal techniques, our suite of tools provide powerful solutions to important design problems, from the very beginning of the design cycle, to the end of the implementation cycle. We call this: "Delivering Verification Confidence".

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Synopsys is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' verification solutions provide proven tools and methodologies that give chip and system development teams a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys also provides a comprehensive methodology for architecting and deploying virtual platforms and FPGA-based ASIC prototypes for speeding chip verification and enabling early software development.

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Zazz from Zocalo Tech is software for creating, using and reusing assertions. Zazz has been architected and developed from the ground up with one goal in mind… increasing productivity for engineers adopting and utilizing Assertion Based Design and Assertion Based Verification. Zocalo will introduce the first release of Zazz that supports Accellera's Open Verification Library (OVL) and Cadence's Incisive Assertion Library (IAL).

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Wednesday Lunch	cādence™
Thursday Lunch	Mentor Graphics®

ADDITIONAL MEETING

North American SystemC Users Group Meeting (NASCUG)

www.nascug.org

Tuesday, February 24 8:30am - 12:00pm Monterey/Carmel Room

The North American SystemC Users Group (NASCUG) provides a unique forum for sharing SystemC experiences among business, research and universities, while influencing the growth and evolution of SystemC standards. A central component of the NASCUG meeting is a number of 20 minute user experience presentations discussing practical design, modeling and verification techniques using SystemC. Several "how-to" presentations will focus on clarifying poorly understood or misused SystemC features.

TOPICS include:

- Architectural Modeling with SystemC
- Transaction-Level Modeling and TLM-2.0
- SystemC Analog/Mixed-signal (AMS) extensions
- Software Co-Design with SystemC
- Verification Techniques using SystemC
- Integrating SystemC into the Design Flow
- SystemC Tool Flows and Methodologies
- SystemC Language Development

Registration is FREE for industry professionals. Find out more at www.nascug.org

NASCUG operates independently but works in collaboration with the Open SystemC Initiative (OSCI) to provide open forums for promoting information exchange. Our goal is to make SystemC end-users more effective through shared knowledge and collaboration.

To find out more about OSCI, visit www.systemc.org

Hotel Floorplan

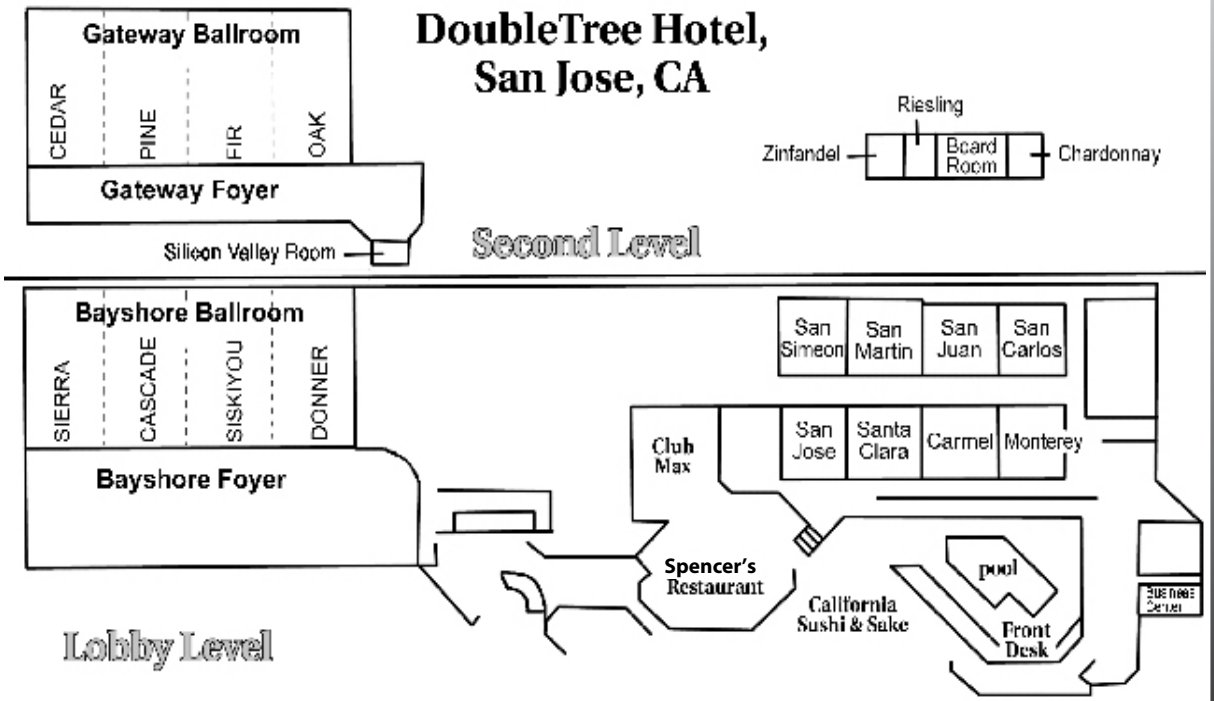
Bayshore Foyer
- Conference Registration

Pine/Ceda
- Tuesday Lunch
- Wednesday Breakfast
- Wednesday Lunch
- Thursday Breakfast
- Thursday Lunch

Oak/Fir
- Tuesday Tutorials
- WednesdayTechnical Sessions
- Wednesday Keynote
- Wednesday Panel

Donner/Sisikiyou/ Cascade
- Thursday Technical Sessions
- Thursday Panel
- 2009 Best Paper Award Presentation

Bayshore Ballroom
- DVCon Expo
- Tuesday Cocktail Reception
- Wednesday Cocktail Reception



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February 23-25, 2010

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