2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCON 2015
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	22%
Standard IC Design	7%
ASIC /SoC Design	33%
DSP Design	4%
Microprocessor/Microcontroller Design	11%
IP Development	16%
Library Development	3%
Analog/Mixed Signal	10%
EDA Methods & Tools	30%
Verification	52%
FPGAs & PLDs	18%
Multi-Chip Modules	3%
PCB Design	4%
Software/Embedded Software	14%
Student	2%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	14%
Engineering Management	15%
Design Engineer	13%
System Architecture	4%
Application Engineer	5%
Marketing	4%
Technical Marketing	3%
Product Marketing	3%
Sales	4%
Research/Academic	2%
CAD	2%
Verification Engineer	27%
Software Engineer	4%
Student	2%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	43%
<1M	8%
1 - 5M	9%
5 - 10M	8%
10M - 50M	30%
50 - 100M	8%
>100M	17%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	52%
VHDL	26%
C/C++	58%
SystemC	21%
SystemVerilog	68%
e	4%
Not Applicable	18%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	52%
OVM	4%
VMM	3%
eRM	1%
SystemC/TLM	5%
Proprietary	8%
Not Involved	28%

FIRST-TIME ATTENDEE

Yes	39%
No	61%