2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCon 2016
ATTENDEE QUESTIONNAIRE RESULTS

ATTENDEES' PRIMARY JOB FUNCTIONS

System Design	20%
Standard IC Design	11%
ASIC /SoC Design	37%
DSP Design	6%
Microprocessor/Microcontroller Design	11%
IP Development	18%
Library Development	4%
Analog/Mixed Signal	13%
EDA Methods & Tools	32%
Verification	58%
FPGAs & PLDs	16%
Multi-Chip Modules	5%
PCB Design	5%
Software/Embedded Software	14%
Student	2%

ATTENDEES' JOB DESCRIPTIONS

Senior Management	14%
Engineering Management	16%
Design Engineer	11%
System Architecture	3%
Application Engineer	5%
Marketing	3%
Technical Marketing	3%
Product Marketing	4%
Sales	4%
Research/Academic	2%
CAD	3%
Verification Engineer	29%
Software Engineer	3%
Student	1%

SIZE IN GATES OF ATTENDEES' CURRENT/LAST DESIGN

Not Applicable	38%
<1M	9%
1 - 5M	8%
5 - 10M	8%
10M - 50M	9%
50 - 100M	78%
>100M	20%

VERIFICATION LANGUAGE USED BY EITHER ATTENDEE OR FUNCTIONAL VERIFICATION TEAM

Verilog	54%
VHDL	19%
C/C++	36%
SystemC	17%
SystemVerilog	72%
e	5%
Not Applicable	17%

VERIFICATION METHODOLOGY USED BY FUNCTIONAL VERIFICATION TEAM

UVM	55%
OVM	3%
VMM	2%
eRM	0%
SystemC/TLM	4%
Proprietary	8%
Not Involved	27%

FIRST-TIME ATTENDEE

Yes	38%
No	62%