Agnisys to showcase Portable Implementation Sequence Generator for PSS Tools and present 'Register Automation using Machine Learning' at DVCON US 2019

San Jose, CA – February 11, 2019 – Agnisys Inc., the leading EDA provider of the industry's most comprehensive solution for Design and Verification of the Hardware/Software Interface (HSI), will present a paper on two machine learning applications: *Register Automation* and *SystemVerilog Assertions,* at DVCon US 2019 February 25-28, 2019. Additionally, Agnisys will introduce the new integration of ISequenceSpec™ with Portable Test and Stimulus Standard (PSS) tools, providing a solution that generates implementation sequences mapped within PSS.

By design, PSS does not contain implementation-level detail of the tests, users create the low- level sequences in some way and "stitch" them with the output generated by the PSS processing tool. Users create the test intent using PSS and generate C/UVM models from it, however, the HSI layer is not part of this description.

"As a contributor to the Accellera PSS 1.0, we believe the HSI layer is critical to enabling a truly portable test because the HSI consists of register data, memory maps, interrupts and CPU Instruction Set Architecture (ISA)," said Anupam Bakshi, Agnisys Founder and CEO. *"ISequenceSpec now supports PSS tools. Users are now able to write sequences from a single specification (spreadsheet or txt format) and auto-generate the C/UVM sequences with the corresponding PSS 'exec' blocks."*

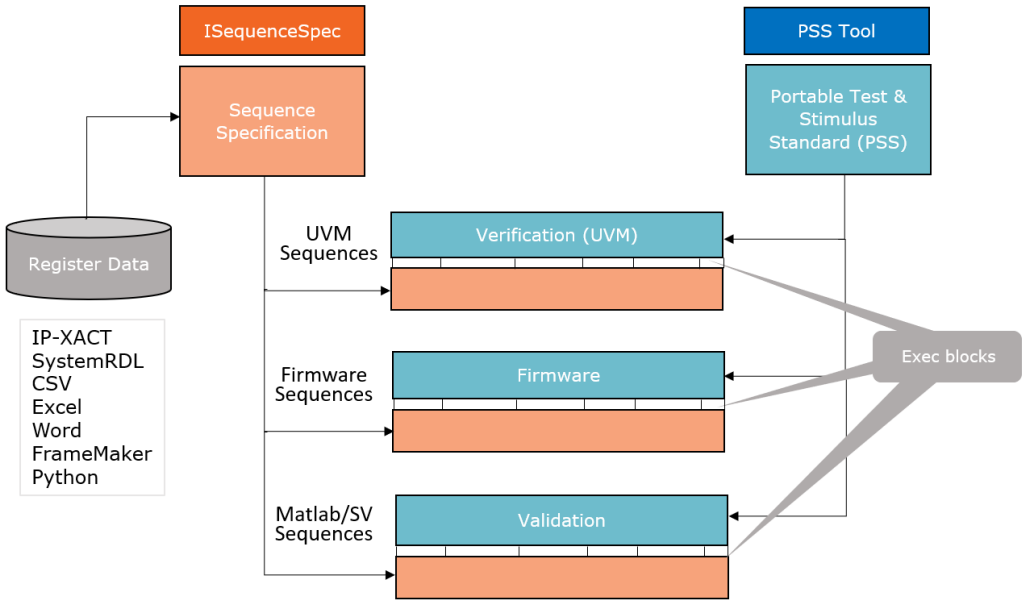

Figure 1: Interface of ISequenceSpec and PSS Tool

Taking part in the conference presentations, Nikita Gulliya, Agnisys R&D Engineer to present:

- Using Machine Learning in Register Automation and Verification
  Paper Presentation – TUESDAY February 26, 3:00pm – 4:30pm | Fir
- In Pursuit of Faster Register Abstract Layer (RAL) Model
  Poster Presentation – TUESDAY February 26, 10:30am – 12:00pm | Gateway Foyer

See Technical Demonstrations of Agnisys HSI solutions at Booth #902:

- IDesignSpec™ – An end-to-end solution for centralizing register design and verification from a golden specification in Word, Excel, IP-XACT or SystemRDL. Auto-generates sign-off quality register RTL code, UVM models, C/C++ headers and HTML/PDF documentation.
- ISequenceSpec™ – An add-on to IDesignSpec where users can define sequences from a single specification and auto-generates portable UVM/C/CSV sequences for simulation, firmware and post-silicon validation. Includes interface with PSS tools for auto-generating UVM/C sequences within 'exec' blocks.
- ARV™ – An add-on to IDesignSpec that auto-generates a complete UVM environment with sequences for RTL simulation and assertions for formal verification, providing 100% functional coverage.

About Agnisys

Agnisys, Inc. is a leading supplier of Electronic Design Automation (EDA) software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for System-on-Chip (SoC) and intellectual property (IP) enabling faster design, verification, firmware, and validation. Based on patented technology and intuitive user interfaces, its products increase productivity and efficiency while eliminating system design and verification errors. Founded in 2007, Agnisys is based in Boston, Massachusetts with R&D centers in the United States and India. www.agnisys.com

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