2012 Design and Verification Conference
Attendee Questionnaire Results

	Percentage
1. Which is your primary design language? (Pick one)	
Verilog	20%
VHDL	5%
C/C++	7%
SystemC	8%
SystemVerilog	51%
Not Applicable	9%

	Percentage
2. Which primary verification language do you use? (Pick one)	
C/C++	13%
e	3%
OpenVera	1%
Verilog	14%
VHDL	4%
SystemC	6%
System Verilog	50%
Not Applicable	9%

	Percentage
3. Which primary verification language do you plan to use for your next design? (Pick one)	
C/C++	10%
e	3%
OpenVera	0%
Verilog	9%
VHDL	3%
SystemC	7%
SystemVerilog	58%
Not Applicable	10%

	Percentage
4. Which verification methodology is used by your functional verification team?	
UVM	32%
OVM	12%
VMM	8%
eRM	1%
SystemC/TLM	5%
Home Grown	12%
Other	7%
I am not involved	23%

	Percentage
5. Which primary property specification (assertion-based verification) language do you use?	
Verilog	26%
VHDL	6%
PSL	4%
SystemVerilog (SVA)	64%

	Percentage
6. What area(s) are you focused on? (Check all that apply)	
Systems Design	10%
Standard ICs	4%
ASICs	15%
DSP Design	3%
Microprocessor/Microcontroller Design	6%
FPGAs & PLDs	8%
Multi-Chip Modules	2%
PCBs	2%
Library Development	2%
Analog/Mixed Signal	4%
EDA Tools	12%
Verification	15%
SOCs	11%
Software/Embedded Software	6%

	Percentage
7. What on-chip buses do you intend to use in the next 12 months?	
AMBA 2.0 AHB/APB	19%
AMBA 3 AXI	20%
OCP 2.0	3%
OCP 2.1	4%
CoreConnect	2%
Others/Proprietary	22%
None	30%

	Percentage
8. What interfaces standards do you expect to use in the next 12 months?	
PCI Express 1.1	5%
PCI Express 2.0	16%
USB 2.0/OTG	8%
USB 3.0	12%
Serial ATA	5%
10G Ethernet	9%
10/100/1G Ethernet	11%
Wireless USB	4%
PCI/PCI-X	6%
CE-ATA	1%
None	23%

	Percentage
9. What is the size in gates of your current/last design? (Pick one)	
Not Applicable	40%
<1M	9%
1 - 3M	7%
3 - 5M	4%
5 - 10M	9%
10M - 50M	14%
>50M	17%

	Percentage
10. How many clock domains do your designs average?	
1	4%
2	5%
2 -5	19%
5 - 10	10%
10 - 20	14%
>20	11%
Not Applicable	37%

	Percentage
11. What is your number one design constraint?	
Low power	38%
Size/density	16%
Performance/throughput	46%

	Percentage
12. What are the two main reasons for your attendance at DVCon?	
Learn new techniques to improve your design process	16%
Learn new methodologies to improve your verification process	26%
Learn about new developments in design tools	19%
Meet and network with other engineers in the industry	22%
Learn about industry in general	17%

	Percentage
13. Which category most closely describes your job description? (Pick one)	
Senior Management	15%
Engineering Management	16%
Design Engineer	15%
System Architecture	2%
Application Engineer	4%
Marketing	4%
Technical Marketing	4%
Product Marketing	4%
Sales	2%
Research/Academic	3%
CAD	3%
Verification Engineer	24%
Software Engineer	4%