DVCon
Design & Verification Conference & Exhibition

2011 Design and Verification Conference
Attendee Questionnaire Results

	Count	Percents
Which is your primary design language? (Pick one)		
Verilog	343	48%
VHDL	50	7%
C/C++	91	13%
SystemC	66	9%
SystemVerilog	168	23%
	718	100%
Which primary verifcation language do you currently use? (pick one)		
C/C++	116	16%
e	23	3%
OpenVera	11	2%
Verilog	129	18%
VHDL	25	3%
SystemC	69	10%
System Verilog	342	48%
	715	100%
Which primary verification language do you plan to use for your next design? (Pick one)		
C/C++	95	13%
e	15	2%
OpenVera	7	1%
Verilog	83	12%
VHDL	20	3%
SystemC	74	10%
SystemVerilog	422	59%
	716	100%
Which primary property specification (assertion-based verification) language do you use or plan to use?		
Verilog	183	27%
VHDL	33	5%
PSL	27	4%
SystemVerilog (SVA)	430	64%
	673	100%
What design area(s) are you focused on? (Check all that apply)		
Systems Design	234	11%
Standard ICs	75	4%
ASICs	312	15%
DSP Design	70	3%
Microprocessor/Microcontroller Design	127	6%
FPGAs & PLDs	189	9%
Multi-Chip Modules	48	2%
PCBs	38	2%
Library Development	43	2%
Analog/Mixed Signal	76	4%
EDA Tools	263	13%
Verification	356	17%
SOCs	243	12%
	2074	100%
What on-chip buses do you intend to use in the next 12 months?		
AMBA 2.0 AHB/APB	203	20%
AMBA 3 AXI	211	21%
OCP 2.0	37	4%
OCP 2.1	60	6%
CoreConnect	25	2%
Others/Proprietary	213	21%
None	263	26%
	1012	100%

	Count	Percents
What standard interface do you expect to use in the next 12 months?		
PCI Express 1.1	93	6%
PCI Express 2.0	243	17%
USB 2.0/OTG	190	13%
Serial ATA	103	7%
10G Ethernet	132	9%
10/100/1G Ethernet	204	14%
Wireless USB	72	5%
PCI/PCI-X	95	7%
CE-ATA	8	1%
None	297	21%
	1437	100%
What is the size in gates of your current/last design? (Pick one)		
Not Applicable	268	37%
<1M	56	8%
1 - 3M	59	8%
3 - 5M	42	6%
5 - 10M	80	11%
10M - 50M	115	16%
>50M	105	14%
	725	100%
How many clock domains do your designs average?		
1	38	5%
2	42	6%
2 -5	206	28%
5 - 10	106	14%
10 - 20	72	10%
>20	51	7%
Not Applicable	226	30%
	741	100%
What is your number one design constraint?		
Low power	257	36%
Size/density	100	14%
Performance/throughput	355	50%
	712	100%
What are the two main reasons for your attendance at DVCon?		
Learn new techniques to improve your design process	263	18%
Learn new methodologies to improve your verification process	404	28%
Learn about new developments in design tools	252	18%
Meet and network with other engineers in the industry	291	20%
Learn about industry in general	230	16%
	1440	100%
Which category most closely describes your job description? (Pick one)		
Senior Management	115	16%
Engineering Management	125	17%
Design Engineer	114	15%
System Architecture	29	4%
Application Engineer	31	4%
Marketing	35	5%
Technical Marketing	39	5%
Product Marketing	17	2%
Sales	26	4%
Research/Academic	29	4%
CAD	23	3%
Verification Engineer	158	21%
	741	100%

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