Monday, March 3 • 5:00 - 7:00pm
Exhibit Floor

• Attend the Booth Crawl
• Get Automatically Entered Into a Drawing For a $500 Visa Gift Card

Winner announced Monday - 6:45pm on the exhibit floor!*

1st Annual Booth Crawl

Cocktails & Conversations

Monday, March 3 • 5:00 - 7:00pm
Exhibit Floor

Visit These Participating Company’s Booths:

*The Winner Must Be Present To Win
For DVCon 2014, we have sought to explicitly expand the conference’s focus from simply being on “Design and Verification” to a more specific focus on hot topic areas that are critical to our conference’s attendees, viz.

- System Level Design
- Verification & Validation
- IP Reuse and Design Automation
- Mixed-Signal Design and Verification
- Lower Power Design and Verification

Attendees will find each of these areas addressed in the conference’s sessions with an emphasis on real world solutions to engineers’ real world problems. Indeed, this focus on the users of EDA languages, tools, methodologies and standards continues to be a DVCon hallmark. DVCon 2014 attendees can expect to learn about both practical solutions to their pressing problems, but also to receive a preview of the technologies that will affect them in the near future.

Technical sessions. Once again, the number of submissions far exceeded the number of available program slots. The technical program committee has selected the highest quality proposals and apportioned them into 12 paper sessions and a poster session. Attendees will vote on the best paper, which will be announced after the final technical session on Wednesday.

Tutorials. There will be twelve tutorials given this year—five on Monday built around Accellera System Initiative standards, and seven from vendors on Thursday. The Thursday tutorial sessions have particularly been expanded, with each of the three largest EDA vendors giving two tutorials spanning the entire day.

Exhibits. The vendor exhibits on Tuesday and Wednesday allow attendees to meet with forty vendors to get in-depth demonstrations of products, solutions and services in the design and verification areas. One change this year is the addition of a “booth crawl” on Monday evening. This crawl will feature cocktails and conversations in a casual environment with the participating DVCon exhibitors. Participants in this crawl will be entered in a drawing for a $500 ViSa gift card.

Keynote. This year’s keynote “An Executive View of Trends and Technologies in Electronics” will be given by Lip-Bu Tan, Chairman and CEO of Cadence Design Systems. Lip-Bu will discuss the relationships between market trends, opportunities, and challenges, and show how new design technologies are an essential element of continuing innovation.

Panels. Two panel sessions will take place on DVCon Wednesday. In the morning there will be a panel entitled “Is Software the Missing Piece In Verification?”. The “Industry Leaders” panel entitled “Did We Create the Verification Gap?”, held later on Wednesday will contain luminaries from both the Design and Verification world. Finally, the conference sponsor, the Accellera Systems Initiative, will host a special lunch panel on Monday entitled, “The Future of Mixed Signal Verification: From Manual Simulations to Full Regression?”. In this panel, experts from User companies will discuss emerging techniques that can enable the digital-centric mixed-signal community to reach their next level of verification.

Finally, I thank all attendees for coming to DVCon 2014. I realize that you are taking valuable time away from your day job to attend DVCon. With this in mind, the DVCon Steering committee has worked overtime to ensure a high return on the time you invest at DVCon. Of course, we realize that there is always room for improvement, and welcome your feedback in our attendee survey. We are particularly interested in your reaction to the new DVCon focus on both Design and Verification.
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YOUR WEEK AT DVCON!

>> Registration Hours:
Monday, March 3:  7:30am to 7:00pm
Tuesday, March 4:  7:30am to 6:30pm
Wednesday, March 5:  7:30am to 6:30pm
Thursday, March 6:  7:30am to 4:00pm

>> Expo Hours:
Monday, March 3 5:00pm to 7:00pm
Tuesday, March 4 2:30pm to 6:00pm
Wednesday, March 5 2:30pm to 6:00pm

>> Parking Instructions:
Local Attendees are to scan their parking ticket at the designated DVCon validation area (Bayshore Foyer). The scanner will beep 3 times to notify the attendee has validated their tickets at the group discounted rate.

There are two pay stations inside the hotel. One is located near the convention entrance (Bayshore Foyer) side and this machine accepts both cash and credit card. The second pay station is located near the guest elevators near the South Parking Lot. This machine accepts only Cash. **Overnight self parking is $7.00 per day/per car with no in/out privileges.**

ENJOY FREE WI-FI AT DVCON!

>> Connect to the Conference Wi-Fi via:
Wi-Fi SSID: DVCON2014
No Password Required.

DVCON TUTORIALS & PROCEEDINGS DISTRIBUTION

DVCon Proceedings and tutorials will be delivered electronically online via a username and password.

To access: http://proceedings.dvcon.org
Username = Email address
Password = Registration ID (on your badge)

Please refer to your registration receipt to access the files you are eligible to view.
TWITTER: @DVCON

Follow @DVCon on Twitter and get hourly conference announcements. Also, tweet about your experience and highlights at the conference! #DVCon

BEST PAPER & POSTER VOTING INSTRUCTIONS

As All Access, Conference Only and One-Day only registrants, you are entitled to vote for the “DVCon Best Paper and Poster” awards. The Attendees are the judges!

Enjoy the convenience of voting from your PC and mobile device.

Just Follow These Steps

1. Go to www.vote.dvcon.org
2. Enter your Badge ID & First Name
3. Vote on the papers and posters you have attended
4. See the recipients at 5:00pm on Wednesday, March 5th, in the Oak/Fir Ballroom following the panel

Best Paper & Poster Voting - FAQ

Q: I accidentally voted on a paper that I did not mean to. Can I redo my vote?
A: Yes, you can change your vote on any paper or poster, at anytime before 3:45pm on Wednesday, March 5.

Q: The online voting shows that I have voted on papers/posters which I did not vote on. What does this mean, and how do I undo it?
A: This means that at some point your Badge ID voted on those papers/posters. If you suspect someone else is using your Badge ID you should go to the Registration Desk to be assigned a new ID.
Accellera Systems Initiative, the proud sponsor of DVCon, is an independent organization with the mission to provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process. We collaborate with our community of members to deliver the standards that lower the cost of designing commercial EDA, IC and embedded systems solutions. As a result of its partnership with the IEEE, Accellera standards are transferred to the IEEE Standards Association for formalization and ongoing change control.

Accellera Systems Initiative: A New Synergy for Standards

System, software, and semiconductor design are converging to meet the increasing challenges to create complex integrated circuits and systems on chips. This convergence has brought to the forefront the need for a single organization to facilitate the creation of system-level, semiconductor design and verification standards. Accellera addresses the needs of the system and semiconductor designers who must find new and smarter ways to create and produce increasingly complex chips. The organization is creating more comprehensive standards that benefit the global electronic design community.

Membership

Accellera’s members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry.

For a full list of technical activities that are supported by Accellera and for information on how to join us, please visit our website at www.accellera.org.
Accellera wishes to recognize the outstanding achievements of its Working Group members by selecting an exceptional contributor to our standards development process as a recipient of the Accellera Technical Excellence Award.

This third annual award recognizes major contributions to the development of Accellera standards. Examples of such contributions may include leadership in standardization of new technologies, assuring achievement of standards development goals, and identifying opportunities to better serve the needs of the industry through standards.

Any member of an Accellera Working Group is eligible for the award. Candidates are nominated by the Working Group Chairs and are endorsed and selected by the Accellera Technical Committee.

The recipient of this year’s award will be announced at the Accellera luncheon on Monday, March 3.
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**Mark Azadpour**
Western Digital

**Dan Benua**
Synopsys, Inc.

**Shalom Bresticker**
Intel Corp.

**Clifford Cummings**
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**Stuart Sutherland**
Sutherland Hdl, Inc.

**Robert Troy**
On Semiconductor

**Greg Tumbush**
Tumbush Enterprises, LLC
### TUTORIAL 1: UVM – What’s Now and What’s Next
Oak Ballroom

### TUTORIAL 2: Using UPF for Low Power Design and Verification
Fir Ballroom

**12:15 - 1:45pm - SPONSORED LUNCHEON**

Accellera: State of the Standards

Accellera Technical Excellence Award Presentation

The Future of Mixed Signal Verification:
From Manual Simulations to Full Regression?
Pine/Cedar Ballroom

**2:00 - 5:00pm**

### TUTORIAL 3: Case Studies in SystemC
San Martin/San Simeon Room

**2:00 - 5:30pm**

### TUTORIAL 4: Experience the Next "Wave" of Analog and Digital Signal Processing Using SystemC AMS 2.0
Oak Ballroom

**2:00 - 5:00pm**

### TUTORIAL 5: OCP: The Journey Continues
Fir Ballroom

## 5:00 - 7:00pm - BOOTH CRAWL!

NEW THIS YEAR!! You won’t want to miss the inaugural DVCon Booth Crawl on the exhibit floor. Cocktails and conversations in a casual environment with the DVCon exhibitors. Mingle from booth to booth while enjoying food and drinks provided by the exhibitors.

By attending the Booth Crawl you’ll be automatically entered into a drawing for a $500 VISA gift card. The winner must be present to win and will be announced Monday night.

### EXHIBIT HOURS: 5:00 - 7:00pm - Bayshore Ballroom

Parking: There are two pay stations inside the hotel. One is located near the convention entrance (Bayshore Foyer) side and this machine accepts both cash and credit card. The second pay station is located near the guest elevators near the South Parking Lot. This machine accepts only Cash. Overnight self parking is $7.00 per day/per car with no in/out privileges.
Monday, March 3

Tutorial 1 - UVM - What’s Now and What’s Next

Oak Ballroom 9:00am - 12:00pm

Organizers:
- Tom Alsop - Intel Corp.
- Yatin Trivedi - Synopsys, Inc.
- Adam Sherer - Cadence Design Systems, Inc.

The Universal Verification Methodology (UVM) has experienced great adoption and growth throughout the industry since its initial release as an Accellera standard 3 years ago. Verification engineers, EDA suppliers, service providers, and others throughout the electronics industry are actively creating verification environments following the UVM principles. Concepts like stimulus generation based on sequences, test execution using phases, communication based on transaction-level modeling (TLM), and the introduction of a register layer, all have significantly contributed to the maturity of functional verification practices.

The presenters will share their experiences on both pragmatic topics that can be applied on UVM 1.1 and advanced topics for the next update of the standard. This tutorial will assume SystemVerilog language knowledge when discussing technical content and presenting detailed examples. Among the topics will be sequence creation, register layer use (both beginner and advanced), TLM-based communication, test execution using run-time phases, and messaging enhancements. All verification engineers - from those just starting to work with the UVM to those with years of experience - will gain new knowledge from the tutorials.

Speakers:
- Thomas Alsop - Intel Corp.
- John Aynsley - Doulos
- Shawn Honess - Synopsys, Inc.
- Tom Fitzpatrick - Mentor Graphics Corp.
- Uwe Simm - Cadence Design Systems, Inc.
Tutorial 2 - Using UPF for Low Power Design and Verification

Organizers:
- Erich Marschner - Mentor Graphics Corp.
- John Biggs - ARM Ltd.

This tutorial presents the latest information on the Unified Power Format (UPF), based on IEEE Std 1801-2013 UPF which was released in late May of last year. Beginning with a review of the concepts, terminology, commands, and options provided by UPF, it will cover the full spectrum of UPF capabilities and methodology, from basic flows through advanced applications, with particular focus on incremental adoption of UPF. Tutorial attendees will come away with a thorough understanding of UPF usage in low power design and verification flows and its role in energy aware system design.

Speakers:
- Erich Marschner - Mentor Graphics Corp.
- John Biggs - ARM Ltd.
- Sushma Honnavara-Prasad - Broadcom Corp.
- David Cheng - Cadence Design Systems, Inc.
- Shreeram Ramachandra - Synopsys, Inc.
- Nagu Dhanwada - IBM Corp.
The Future of Mixed Signal Verification: From Manual Simulations to Full Regression?

In just a decade, the landscape of mixed signal design has drastically changed. While co-simulations between a digital and analog solver have evolved into a more complex mixed signal verification environment, there is a clear need today for advanced debugging features and technologies to help the digital-centric mixed-signal community to reach next level of verification. While the future and unification of mixed signal verification is unclear due to the large diversity of use models and needs in the industry, new technologies and trends are emerging.

The invited panelists will present and discuss those emerging techniques that would enable the digital-centric mixed-signal community to reach their next level of verification. Among topics, we will cover:

• New behavioral modeling needs and standards
• Digital verification methodologies applied to mixed signal
• Debugging/regression environment

With a good mixture of technical mixed-signal competences in the panel, practical guidance and experiences are shared with are valuable for the audience.

Panelists:

Scott Little - Intel Corp.
Scott Morrison - Texas Instruments, Inc.
Neyaz Khan - Maxim Integrated
Martin O’Leary - Qualcomm, Inc.
Organizer:
Yatin Trivedi - Synopsys, Inc.

For more than a decade, SystemC has been used by system architects and design engineers. In more recent times Transaction Level Modeling (TLM2) and virtual prototyping have been an integral part of rewriting some of the models and enhancing the design and verification methodologies from earlier efforts. They have continued to deploy evolving methodologies in new application areas such as radio base station and network processors to bring-up software months ahead of the traditional approach. Other users have attempted to bridge the interoperability gap between SystemC and Universal Verification Methodology (UVM) based on SystemVerilog and other HDLs. In this tutorial, hands-on users and tool developers share their recent experience and describe advanced methodologies that have helped them achieve significant benefits. A few of the most useful features introduced with SystemC 2.3.0 will be presented and provide code examples that you can take away and start to use for yourself.

Speakers:
- John Aynsley - Doulos
- Henrik Svensson - Ericsson
- Martin Barnasconi - NXP Semiconductors
- Donald Cramb - Synopsys, Inc.
- John Stickley - Mentor Graphics Corp.
Today’s embedded systems and SoCs contain more and more physical interface IPs (e.g. USB, PCIe, DDR, SATA and HDMI) and mixed-signal IP (e.g. Sigma-delta-ADCs, DACs and PLLs) which directly interact with the digital HW/SW subsystems. For example, many of these mixed-signal IPs are registered-controlled and can be configured and calibrated via the on-chip processor.

Furthermore, while data-rates continue to increase, design of these high-speed peripherals requires inclusion of the analog/mixed-signal behavior in the overall signal processing chain to guarantee error-free transmission and reception over the physical channels. This requires new means to model and simulate the algorithms and signal processing capabilities of these peripherals, in combination with the HW/SW subsystems at functional and architecture level. Especially for this purpose, the SystemC language standard has been extended with powerful mixed-signal and signal processing modeling features to tackle the challenges in heterogeneous electronic system-level design and verification.

This tutorial will be conducted as a true “hands-on” session: after a basic introduction on the SystemC AMS 2.0 modeling concepts and methodology, everyone is encouraged to actually create models, run simulations and look at waveforms! To facilitate this, information distribution will be made available for the attendees, including a fully prepared system-level modeling environment, which they can run immediately on their own laptop.

In an interactive way, presentations and “labs” will be alternated introducing both analog and digital signal processing exercises, giving the attendees a valuable introduction of the existing and new features of SystemC AMS. Examples are the creation of analog filters, analog-to-digital converters and completion of a transceiver system using digitally modulated signals.

This highly technical tutorial targets system engineers, integrators, architects and verification engineers active in industrial projects where analog and digital signal processing functionality comes together and where interoperability between mixed-signal and HW/SW subsystems becomes apparent. Note that the tutorial does not target analog/mixed-signal circuit-level and mixed transistor/RTL modeling; instead, it will focus on abstract mixed-signal modeling for system-level design and verification. Therefore experience with algorithm and C/C++/SystemC languages is highly preferred.

So in case you are interested to experience the next ~wave~ of analog and digital signal processing using SystemC AMS? Join us at DVCon 2014!

Speakers and trainers in this workshop are recognized leaders in the field of mixed-signal system-level modeling:

- Karsten Einwich, Fraunhofer IIIS/EAS Dresden, Germany - Creator of the SystemC AMS compliant proof-of-concept implementation
- Francois Pêcheux, University Pierre et Marie Curie, Paris, France - Leader in scientific innovation using SystemC AMS for RF, communication and biomedical applications

Similar sessions have been organized in Europe at major conferences and events. The organizer and speakers would like to bring the success of SystemC AMS in Europe to other regions of the world.

**Speakers:**

- **Karsten Einwich** - Fraunhofer IIIS
- **Francois Pêcheux** - Univ. Pierre et Marie Curie
- **Martin Barnasconi** - NXP Semiconductors
- **Torsten Mähne** - Univ. Pierre et Marie Curie
This tutorial will present the past, present and future of the Open Core Protocol IP interface socket standard, which was transferred to Accellera in October, 2013. The tutorial will provide some history and a basic introduction to the OCP Specification itself, and then discuss a variety of topics crucial to the use of OCP in SoC designs: verification IP support, TLM 2.0 SystemC support and IP-XACT support. The tutorial will close with a discussion of future needs in IP core interfacing, and where future version of the OCP standard may play a role.

Speakers:
- Drew Wingard - Sonics, Inc.
- Steve McMaster - Synopsys, Inc.
- Herve Alexanian - Sonics, Inc.
- Prashant Karandikar - Texas Instruments, Inc.
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TUESDAY AGENDA

8:30 - 9:00am - DVCON 2014 OPENING SESSION

General Chair - Stanley J. Krolkoski, Ph.D.
Cadence Design Systems, Inc.
Oak Ballroom

9:00 - 10:30am

SESSION 1: Advanced Design and Verification
Oak Ballroom
SESSION 2: Formal and Semi-Formal Techniques
Fir Ballroom
SESSION 3: Hw/Sw Co-Verification
San Jose/Santa Clara Room

10:30am - 12:00pm - POSTER SESSION

POSTER SESSION - Gateway Foyer

12:00 - 1:15pm - SPONSORED LUNCHEON

System to Silicon Verification - Challenges & Solutions
Pine/Cedar Ballroom

2:00 - 2:30pm - KEYNOTE ADDRESS

Lip-Bu Tan, President & CEO
Cadence Design Systems, Inc.
An Executive View of Trends and Technologies in Electronics
Oak Ballroom

EXHIBIT HOURS: 2:30 - 6:00pm - Bayshore Ballroom

It’s about meeting people, education & solving your design questions.

3:00 - 5:00pm

SESSION 4: Advance Methodologies and Testbenches - I
Oak Ballroom
SESSION 5: Mixed-Signal Design and Verification
Fir Ballroom
SESSION 6: Low Power Design and Verification
San Jose/Santa Clara Room

5:00 - 6:00pm - NETWORKING RECEPTION

Lively discussion partnered with light hors d’oeuvres and cocktails.

Parking: There are two pay stations inside the hotel. One is located near the convention entrance (Bayshore Foyer) side and this machine accepts both cash and credit card. The second pay station is located near the guest elevators near the South Parking Lot. This machine accepts only Cash. Overnight self parking is $7.00 per day/per car with no in/out privileges.
**Session 1 - Advanced Design and Verification**

Oak Ballroom 9:00 - 10:30am

**Chair:** Charles Dawson - Cadence Design Systems, Inc.

1.1 Advancing System-Level Verification Using UVM in SystemC
   Martin Barnasconi - NXP Semiconductors
   François Pêcheux - Univ. Pierre et Marie Curie
   Thilo Vörtler - Fraunhofer IIS

1.2 Synthesizable SystemVerilog — What ASIC and FPGA Synthesis Compilers Support in the SystemVerilog-2012 Standard
   Stuart Sutherland - Sutherland HDL, Inc.
   Don Mills - Microchip Technology, Inc.

1.3 Using SystemVerilog Interfaces and Structs for RTL Design
   Nihar Shah, Tom Symons - Oracle Corp.

**Session 2 - Formal and Semi-Formal Techniques**

Fir Ballroom 9:00 - 10:30am

**Chair:** Erik Seligman - Intel Corp.

2.1 Sign-off With Bounded Formal Verification Proofs
   NamDo Kim, Junhyuk Park - Samsung Electronics Co., Ltd,
   HarGovind Singh, Vigyan Singhal - Oski Technology, Inc.

2.2 A Formal Verification App Towards Efficient Chip-Wide Clock Gating Verification
   Syed Suhaib, Scott Fields, Prosenjit Chatterjee - NVIDIA Corp.

2.3 Practical Approach Using A Formal App to Detect X-Optimism-Related RTL Bugs
   Shuqing Zhao, Shan Yan, Yafang Feng - Broadcom Corp.

**Session 3 - Hw/Sw Co-Verification**

San Jose/Santa Clara Room 9:00 - 10:30am

**Chair:** Joanne DeGroat - Ohio State Univ.

3.1 Tried and Tested Speedups for Software-Driven SoC Simulation
   Gordon Allan - Mentor Graphics Corp.

3.2 Learning From Advanced Hardware Verification for Hardware Dependent Software
   Simond Davidmann - Imperas, Inc.

3.3 “C” You on the Faster Side: Accelerating SV DPI Based Co-Simulation
   HariVinodh Balisetty - Broadcom Corp.
   Amit Sharma - Synopsys, Inc.
   Parag Goel - Synopsys (India) Pvt. Ltd.
**Poster Session** - Poster Session

**Gateway Foyer** 10:30am - 12:00pm

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<td><strong>1P.12 Supercharge Your Verification Using Rapid Expression Coverage as the Basis of a MC/DC-Compliant Coverage Methodology</strong></td>
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Poster Session Cont.

1P.13 *So You Think You Have Good Stimulus: System-Level Distributed Metrics Analysis and Results*
Andreas Meyer - Mentor Graphics Corp.
Alan Hunter - ARM Ltd.

1P.14 *UVM SchmooVM – I Want My C Tests!*

1P.15 *Verification Mind Games - How to Think Like a Verifier*
Jeffrey Montesano, Mark Litterick - Verilab, Inc.

1P.16 *Easier UVM - Coding Guidelines and Code Generation*
John Aynsley, Christoph Sühnel - Doulos

1P.17 *VIP Shielding*
Jeremy Ridgeway, Karishma Dhruv - LSI Corp.

1P.18 *Bringing Regression Systems Into the 21st Century*
David Crutchfield - Cypress Semiconductor Corp.
Thomas Ellis - Mentor Graphics Corp.

1P.19 *Are You Really Confident That You Are Getting the Very Best From Your Verification Resources?*
Thom Ellis - Mentor Graphics Corp.
Fritz Ferstl - Univa Corp.

1P.20 *Connecting the Dots: Application of Formal Verification for SoC Connectivity*
Bin Ju - Cadence Design Systems, Inc.

1P.21 *Generation of Constraint Random Transactions for Verification of Mixed-Signal Blocks*
Alexander Rath, Sebastian Simon, Volkan Esen, Wolfgang Ecker - Infineon Technologies AG

1P.22 *Metric Driven Mixed-Signal Verification Methodology and Practices for Complex Mixed-Signal ASSPs*
Frank Yang, Andy Sha, Morton Zhao - Analog Devices, Inc.
Yanping Sha - Cadence Design Systems, Inc.

1P.23 *Is Your Power Aware Design Really X-Aware?*
Durgesh Prasad, Jitesh Bansal - Mentor Graphics Pvt. Ltd., India

1P.24 *Architectural Evaluation of a Programmable Accelerator for Baseband, Phy and Video Applications using High Level Synthesis*
Andy Fox - Really Useful Software and Hardware Company
Steven Anderson - Forte Design Systems

1P.25 *Equivalence Validation of Analog Behavioral Models*
Manish Karna, Hardik Parekh, Mohit Jain - STMicroelectronics
Atul Pandey, Sandeep Mittal - Mentor Graphics Corp.
Yet again, the industry is at the edge of significant changes to verification. Escalating challenges like verification of performance, how power budgets are met and how hardware and software interact are pushing the envelope for more efficient verification and verification re-use across abstraction levels and different verification engines. Join us for a System-to-Silicon Verification Luncheon at DVCon in San Jose.

Industry experts including EDA visionary and investor James Hogan will present and debate the direction of system verification. Selected users will detail how they’ve solved some of today’s hardest challenges in system and silicon verification. This luncheon will provide an unprecedented opportunity to hear first hand from peers and colleagues how they tackled the toughest verification issues, to network with your peers, and to collaborate with industry experts. Whether your challenge relates to performance, productivity, or accuracy, this luncheon will present you with new perspectives on improving quality while meeting demanding product schedules.

Speaker:

James Hogan - Consultant
**Keynote: An Executive View of Trends and Technologies in Electronics**

**Oak Ballroom**  
2:00 - 2:30pm

The Semiconductor Revolution continues to drive tremendous economic growth more than 50 years after it began. Today’s major trends - like cloud computing, wearable computing, and the internet of things - are fueled by innovations in product design using advanced semiconductors.

But rapid market trends bring increasing time-to-market pressures that threaten to stifle innovation. The technical challenges of SoC design for advanced process nodes, as well as system issues like communications performance, data security, and ultra-low-power design, create increased complexity and risk. From a business standpoint, the cost of developing the software is becoming the biggest factor in SoC design, followed by the cost of verifying everything - including the software.

One of the ways the electronics industry addresses these challenges is through improvements in design technology. The EDA industry, including Cadence, is investing billions of dollars to develop new design technologies and methodologies to keep the semiconductor industry moving forward. In this keynote, Lip-Bu Tan will discuss the relationships between market trends, opportunities, and challenges, and show how new design technologies are an essential element of continuing innovation.

Lip-Bu Tan has served as President and CEO of Cadence Design Systems, Inc. since January 2009 and has been a member of the Cadence Board of Directors since February 2004. He also serves as chairman of Walden International, a venture capital firm he founded in 1987. Prior to founding Walden, Tan was Vice President at Chappell & Co. and held management positions at EDS Nuclear and ECHO Energy.

He serves on the Board of Directors of both the Electronic Design Automation Consortium (EDAC) and the Global Semiconductor Association (GSA), as well as the boards of Ambarella Inc., SINA, and Semiconductor Manufacturing International Corp. He also serves on the Board of Trustees and the School of Engineering Dean’s Council at Carnegie Mellon University (CMU), and the College of Engineering Advisory Board at University of California Berkeley.

Tan received an M.S. in nuclear engineering from the Massachusetts Institute of Technology, an MBA from the University of San Francisco, and a B.S. from Nanyang University in Singapore.
Session 4 - Advance Methodologies and Testbenches - I

Oak Ballroom  3:00 - 5:00pm

Chair: Mark Azadpour - Western Digital Corp.

4.1 SystemVerilog Interfaces for Verification Cookbook
Paul Egan, Kathleen Otten - Rockwell Automation, Inc.

4.2 Determining Test Quality Through Dynamic Runtime Monitoring of SystemVerilog Assertions
Kelly Larson - NVIDIA Corp.

4.3 SystemVerilog, Batteries Included: A Programmer’s Utility Library for SystemVerilog
Jonathan Bromley, André Winkelmann - Verilab, Inc.

4.4 Advanced Functional Verification Methodology Using UVM for complex DSP Algorithms in Mixed Signal RF SoCs
Srinivas Aluri - Texas Instruments, Inc.
Neyaz Khan - Maxim Integrated

Session 5 - Mixed-Signal Design and Verification

Fir Ballroom  3:00 - 5:00pm

Chair: Dan Benua - Synopsys, Inc.

5.1 Automated Comparison of Analog Behavior in a UVM Environment
Sebastian Simon, Alexander Rath, Volkan Esen, Wolfgang Ecker - Infineon Technologies AG

5.2 Digitizing Mixed Signal Verification: Digital Verification Techniques Applied to Mixed Signal and Analog Blocks and System Level Verification
David Brownell, Courtney Schmitt - Analog Devices, Inc.

5.3 Efficient SoC Level Mixed Signal Frontend Verification Using WREAL Models
Anu Marisha, Nayana Prakash, Rajesh Tiwari - Texas Instruments India Pvt. Ltd.
Udit Kumar - Texas Instruments, Inc.
Vijay Birange - Cadence Design Systems, Inc.

5.4 Interpreting UPF For A Mixed-Signal Design Under Test
Kenneth Bakalar, Eric Jeandeau - Mentor Graphics Corp.
Session 6 - Low Power Design and Verification

San Jose/Santa Clara Room  3:00 - 5:00pm

Chair: Neyaz Khan - Maxim Integrated

6.1 An Expert System Based Tool for Pre-design Chip Power Estimation
Bhanu Singh, Arunprasath Shankar, Chris Papachristou - Case Western Reserve Univ.

6.2 Stepping Into UPF 2.1 World: Easy Solution to Complex Power Aware Verification
Amit Srivastava, Madhur Bhargava - Mentor Graphics Pvt. Ltd., India

6.3 Power Estimation Techniques – What to Expect, What Not to Expect
Prakash Parikh - Qualcomm, Inc.

6.4 Tackling the Challenge of Simulating Multi-Rail Macros in a Power Aware Flow
Krishna Theja Avvaru - Synopsys, Inc.
Himanshu Bhatt, Amol Herlekar - Synopsys (India) Pvt. Ltd.
Vikas Grover, Subhadip Nath - Advanced Micro Devices, Inc.
8:30 - 9:45am - PANEL
Is Software the Missing Piece In Verification?
Oak Ballroom

10:00 - 11:30am
SESSION 7: System-Level Design - II
Oak Ballroom
SESSION 8: Automated Stimulus Generation
Fir Ballroom
SESSION 9: Advance Methodologies and Testbenches - II
San Jose/Santa Clara Room

12:00 - 1:15pm - SPONSORED LUNCHEON
Accelerating Verification
Pine/Cedar Ballroom

1:30 - 3:00pm - PANEL
Did We Create the Verification Gap?
Oak Ballroom

EXHIBIT HOURS: 2:30 - 6:00pm - Bayshore Ballroom
It’s about meeting people, education & solving your design questions.

3:30 - 5:00pm
SESSION 10: Verification Process and Resource Management
Oak Ballroom
SESSION 11: SoC and IP Integration Methods and Tools
Fir Ballroom
SESSION 12: Interoperability of Models and/or Tools
San Jose/Santa Clara Room

5:00 - 6:00pm - NETWORKING RECEPTION
Lively discussion partnered with light hors d’oeuvres and cocktails.

5:00 - 5:15pm - BEST PAPER & POSTER AWARD PRESENTATIONS
2014 Best Paper & Poster Awards Presentation
Oak Ballroom - 5:00 - 5:15pm
Announced by Technical Program Chair, Ambar Sarkar

Parking: There are two pay stations inside the hotel. One is located near the convention entrance [Bayshore Foyer] side and this machine accepts both cash and credit card. The second pay station is located near the guest elevators near the South Parking Lot. This machine accepts only Cash. Overnight self parking is $7.00 per day/per car with no in/out privileges.
Panel: Is Software the Missing Piece In Verification?

Oak Ballroom  
8:30 - 9:45am

Moderator:
Ed Sperling - Semiconductor Engineering

Organizer:
Liz Massingill - Lee Public Relations

System-level verification has become an endemic problem. Verification budgets are stretched with increasing SoC verification complexity, and teams are looking for ways to improve the productivity of their verification efforts. Vendors such as Breker, Mentor and Vayavya are attempting to automate SoC verification through software-driven verification using a variety of approaches. Is software-driven system-level verification a trend that’s expected to grow or is it just hype?

Panelists from different segments of the semiconductor industry will discuss and debate the presumed need, maturity, scalability, and adoptability of software-driven system-level verification tools, as well as what’s needed to get them to mass usability level. In addition, panelists will discuss current approaches to the verification problem and what place this technology has with respect to current verification methodologies such as UVM.

Panelists:
Tom Anderson - Breker Verification Systems, Inc.
Kenneth Knowlson - Intel Corp.
Steve Chappell - Synopsys, Inc.
Sandeep Pendharkar - Vayavya Labs Pvt., Ltd.
Frank Schirrmeister - Cadence Design Systems, Inc.
Mark Olen - Mentor Graphics Corp.
Session 7 - System-Level Design - II

Oak Ballroom 10:00 - 11:30am

Chair: Greg Tumbush - Tumbush Enterprises, LLC

7.1 Wiretap Your SoC: Why Scattering Verification IPs Throughout Your Design Is A Smart Thing To Do
Avidan Efody - Mentor Graphics Corp.

7.2 Environment For Efficient and Reusable SystemC Module Level Verification
Flavia Gontia - Siemens AG

7.3 Complementing EDA with Meta-Modeling and Code Generation
Wolfgang Ecker, Ajay Goyal, Michael Velten - Infineon Technologies AG

Session 8 - Automated Stimulus Generation

Fir Ballroom 10:00 - 11:30am

Chair: Kaiming Ho - Fraunhofer IIS

8.1 Of Camels and Committees: Standards Should Enable Innovation, Not Strangle It
Tom Fitzpatrick, Dave Rich - Mentor Graphics Corp.

8.2 Constraining the Real Problem of Floating Point Number Distributions
Jussi Mäkelä, Martin Fröjd - ARM Ltd.
Adiel Khan - Synopsys, Inc.

8.3 UVM/SystemVerilog Based Infrastructure and Testbench Automation Using Scripts
Prakash Parikh - Qualcomm, Inc.

Session 9 - Advance Methodologies and Testbenches - II

San Jose/Santa Clara Room 10:00 - 11:30am

Chair: Clifford Cummings - Sunburst Design, Inc.

9.1 Advanced UVM Register Modeling - There’s More Than One Way To Skin A Reg
Mark Litterick, Marcus Harnisch - Verilab, Inc.

9.2 UVM Testbench Considerations for Acceleration
Kathleen Meade - Cadence Design Systems, Inc.

9.3 Applying Test-Driven Development Methods To Design Verification Software In UVM-e
Doug Gibson, Michael Kontz - Hewlett-Packard Co.
Sponsored Luncheon - *Accelerating Verification*

**Pine/Cedar Ballroom**  
12:00 - 1:15pm

**Organizer:**  
Rebecca Granquist - Mentor Graphics Corp.

Mentor Graphics invites you to join us for lunch and informative discussion covering the very latest verification challenges, methodologies and techniques that will help you improve your verification performance and productivity.

**Speaker:**  
Stephen Bailey - Mentor Graphics Corp.
According to industry experts, the “Verification Gap” between what we need to do and what we’re actually able to do to verify large designs is growing worse each year. According to these experts, we must do our best to improve our verification methods and tools before our entire project schedule is taken up by verification tasks.

But what if the Verification Gap is actually occurring as a result of continued adoption of industry standard methods. Are we blindly following industry best practices without keeping in mind that the actual point of our efforts is to create a product with as few bugs as possible, as opposed to simply trying to find as many bugs as we can?

Panelists will explore how verification teams interact with broader project teams and examine the characteristics of a typical verification effort, including the wall between design and verification, verification involvement (or lack thereof) in the design and architecture phase, and reliance on constrained random in absence of robust planning and prioritization to determine the reasons behind today’s Verification Gap.

Panelists:
- Janick Bergeron - Synopsys, Inc.
- Jim Caravella - NXP Semiconductors
- Harry Foster - Mentor Graphics Corp.
- John Goodenough - ARM, Ltd.
- Bill Grundmann - Xilinx, Inc.
- Mike Stellfox - Cadence Design Systems, Inc.
Session 10 - Verification Process and Resource Management

Oak Ballroom 3:30 - 5:00pm

Chair: Robert Troy - ON Semiconductor

10.1 Sharing Generic Class Libraries in SystemVerilog Makes Coding Fun Again
Keisuke Shimizu - ClueLogic, LLC

10.2 A Guide to Using Continuous Integration Within the Verification Environment
Gordon McGregor - Nitero, Inc.
Jason Sprott, André Winkelmann - Verilab, Inc.

10.3 An Assertion Based Approach to Implement VHDL Functional Coverage
Susan Eickhoff, Michael Wazlowski - IBM Systems and Technology Group
Tagbo Ekwueme-Okoli - Cadence Design Systems, Inc.
Michael DeBole - IBM Corp.

Session 11 - SoC and IP Integration Methods and Tools

Fir Ballroom 3:30 - 5:00pm

Chair: Stuart Sutherland - Sutherland HDL, Inc.

11.1 Reusing UVM Testbenches in a Cycle Simulator
Kristina Hager - IBM Corp.
Andrew Lynch, Umer Yousafzai - Cadence Design Systems, Inc.

11.2 Leveraging IP-XACT Standardized IP Interfaces for Rapid IP Integration
David Murray, Simon Rance - Duolog Technologies Ltd.

11.3 Accelerated, High Quality SoC Memory Map Verification Using Formal Techniques
Cletan Sequeira, Rajesh Kedia - Texas Instruments India Pvt. Ltd.
Lokesh Babu Pundreeka, Bijitendra Mittra - Cadence Design Systems, Inc.

Session 12 - Interoperability of Models and/or Tools

San Jose/Santa Clara Room 3:30 - 5:00pm

Chair: Harry Foster - Mentor Graphics Corp.

12.1 Multi-Language Verification: Solutions for Real World Problems
Bryan Sniderman - Advanced Micro Devices, Inc.
Vitaly Yankelevich - Cadence Design Systems, Inc.

12.2 Leveraging Formal to Verify SoC Register Map
Abdul Elaydi - Marvell Semiconductor, Inc.
Jose Barandiaran - Cadence Design Systems, Inc.

12.3 Solving Next-Generation IP Configurability
Simon Rance, David Murray, - Duolog Technologies Ltd.

2014 Best Paper & Poster Awards Presentation
Oak Ballroom - 5:00 - 5:15pm
Announced by Technical Program Chair, Ambar Sarkar
Sponsored by: Verilab
**THURSDAY AGENDA**

**8:30am - 12:00pm**

**TUTORIAL 6:** The How To’s of Metric Driven Verification to Maximize Verification Productivity  
Donner Ballroom

**TUTORIAL 7:** Block to System Verification: Smooth Sailing from Simulation to Emulation  
Siskiyou Ballroom

**TUTORIAL 8:** SoC Verification Challenges Offer Opportunities to Take a New Look at Debug  
San Jose/Santa Clara Room

**TUTORIAL 9:** Formally Verifying Security Aspects of SoC Designs  
Carmel Room

**12:30 - 1:45pm - SPONSORED LUNCHEON**

Industry Leaders Verify with Synopsys  
Cascade/Sierra Ballroom

**2:00 - 5:30pm**

**TUTORIAL 10:** Revolutionary Debug Techniques to Improve Verification Productivity  
Donner Ballroom

**TUTORIAL 11:** Formal Verification in Practice: Technology, Methods and Applications  
Siskiyou Ballroom

**TUTORIAL 12:** Optimizing Coverage-Driven Verification  
San Jose/Santa Clara Room

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Metric Driven Verification (MDV) is a productivity enhancement over the tried and true coverage driven verification, for purposes of functional verification of RTL designs. MDV is used by the majority of chip suppliers, but often only for specific parts of a chip, in a somewhat limited way, and mostly in the context of simulation only environments.

Verification is changing, driven by a rapid increase in design size and complexity. There is a new frontier possible, different than the linear trajectory we are on. At its route, functional verification has always been as much about methodology as it is about tools. We see that successful verification projects accommodate three primary factors - human, methodology, and enabling tools.

The scope of this MDV tutorial is ambitious and vast. It will present and demonstrate the major factors of functional verification, from IP level to SOC level, from simulation to acceleration, from practical methodology guidelines at different stages of integration, to human and tool factors essential to be managed. It will cover those specialty domains necessary for final verification sign-off, and be based on real metrics for data driven decision making. Simple decisions like what information should be measured when have a large impact on productivity, and guidelines will be presented based on actual successful verification engagements.

Topping it off will be techniques to reduce decision churn, and how to focus on pertinent data, meaningfully assembled from the reams of data produced from the verification environment. Cadence has matured and extended the MDV Methodology it pioneered in 2004, to address the new challenges and issues discussed above. The methodology and approach is tool independent, and will have significance no matter which vendor’s tools you are using, as the concepts and strategies are universally applicable.

Speakers:

John Nehls - Cadence Design Systems, Inc.
Matt Graham - Cadence Design Systems, Inc.
Mike Stellfox - Cadence Design Systems, Inc.
Eric Melacon - Cadence Design Systems, Inc.
Jose Barandiaran - Cadence Design Systems, Inc.
With exploding design complexity, verification today requires effective use of a combination of tools and techniques together with methodology and a plan. This tutorial will focus on how multiple verification engines including simulation, formal, emulation and FPGA prototyping can be applied to objectives from block to system-level in order to achieve better verification results faster. In this tutorial, methodology is how to do verification using all or most of the tools available today including UVM. Throughout the tutorial, real examples of customer use cases will be described.

The breadth of this tutorial is better reflected in the specific areas of focus, which include:

#1 Starting with a review of the verification objectives and tasks from block to system level and the relevant factors that influence the best choice of verification engine to achieve those objectives.

#2 Planning verification to:

- Maximize reusability of verification IP including protocol BFM, assertion-checkers, coverage monitors and test specifications (stimulus generators).
- Utilize the best engines, technology and automation to achieve high quality results in the shortest amount of time for various classes of objectives.
- Address chip- and system-level verification considerations such as interfacing with peripherals through new, high-speed standards, system-level interconnect, multi-core coherency and software for driving verification or as part of the system to be verified.
- Support early and continuous concurrent software development and validation.

#3 Ensuring quality by tracking closure on verification objectives throughout verification from block- to system-level and across all engines utilized in the verification flow.

Speakers:

Stephen Bailey - Mentor Graphics Corp.
Jim Kenney - Mentor Graphics Corp.
Ellie Burns - Mentor Graphics Corp.
Tom Fitzpatrick - Mentor Graphics Corp.
Larry Cameron - ARRIS Group, Inc.

Tutorial Sponsored by:
Today’s mobile SoCs combine elements of embedded software, many interface and on-chip protocols, not to mention increasing complexity. To verify these SoCs’, teams apply several technologies and approaches to achieve confident tape-out: constrained-random methodologies, coverage analysis, verification IP, low power simulation and analysis, formal technology, SystemC-TLM performance analysis, and so on. Similarly, debug requires a multi-dimensional approach to rapidly find root causes by highlighting key information and enabling users to quickly filter out trivial data.

This session gives an overview of the latest advances in next generation debug technology. It brings together the leading debug and visualization technologies available in Verdi, next generation transaction debug, advanced HW/SW debug technology, the latest in protocol-aware debug and performance analysis available in Protocol Analyzer and advanced checking and monitoring features in verification IP that combine to create a new wave of debug productivity.

This tutorial will use a case study of an ARM-based SoC to illustrate these multi-level capabilities and how they’re used to enable significantly more productive debug and performance validation of complex RTL in the context of embedded software development.

**Demonstrator:**
- Kiran Maiya - Synopsys, Inc.

**Speakers:**
- Bernie Delay - Synopsys, Inc.
- Steve Chappell - Synopsys, Inc.
- Lance Tamura - Synopsys, Inc.
With every new report of a security breach of an industrial or consumer system, the demand to verify the security features of system-on-chip (SoC) hardware that secure operating systems rely on continues to increase. Complex SoCs, such as those for cell phones, game consoles, medical devices, vehicles, and servers contain secure information that’s valuable for unauthorized parties to exploit. The potential business loss, both direct and indirect, is large - let alone the potential for life threatening, safety-related consequences.

Unfortunately, verifying whether secure information stored in hardware can be leaked is hard to achieve with conventional RTL validation methods. Manual inspection by experts doesn’t scale; and simulation-based or emulation approaches rely on the inconsistent hacking abilities of the verification engineers. Indeed, the problem calls for an exhaustive, formal approach. Thus, in this tutorial we will show how formal analysis can be applied to this area.

Note that a key point we will demonstrate is that security requirements are not easily expressible by regular SV assertions; so it’s not practical to achieve validation with standard formal verification tools. Consequently, we will show how new formal technology and a methodology can be employed to verify the robustness of secure data access and the absence of functional paths touching secure areas of a design. Specifically, using a new Security Path Verification formal app we will show how to specify the security paths and perform an exhaustive verification based on our special path sensitization technology, leverage automatic connectivity abstraction, and path divide-and-conquer search.

All of the above will be demonstrated in the context of several real-world customer case studies.

Speakers:

Victor Markus Purri - Jasper Design Automation, Inc.
Lawrence Loh - Jasper Design Automation, Inc.
Sponsored Luncheon - *Industry Leaders Verify with Synopsys*

Cascade/Sierra Ballroom  
12:30 - 1:45pm

**Moderator:**  
*Michael Sanie - Synopsys, Inc.*

Synopsys has worked with SoC leaders to define and deploy breakthrough technologies that not only increase the speed and throughput of verification (effectively lower the IT cost of verification) but also offer innovative approaches to avoid bugs altogether, detect them as early as possible and debug more efficiently. At this luncheon, you will hear industry experts share their viewpoints on what is driving SoC complexity, how their teams have achieved success, how you can apply their insights on your next project as well as discussions about the latest developments in the verification landscape and advanced technology.
Tutorial 10 - Revolutionary Debug Techniques to Improve Verification Productivity

Donner Ballroom  2:00 - 5:30pm

Organizer:
Kishore Karnane - Cadence Design Systems, Inc.

Still debugging using older conventional methods such as printf? Class-based software-oriented environments are best debugged using interactive debug techniques. Traditional post-process debug techniques can be valuable; however, many limitations, like lack of interactive source-level stepping, make debugging difficult.

Cadence has integrated the best of both worlds: post-process and interactive debug capabilities in a novel multi-language, “interactive” post-process debug solution that can help you fix bugs in minutes instead of hours or days. So, what’s this “interactive” post process debug stuff anyways? It is a combination of interactive and post process debug integrated into a single debug environment. In other words, the designer and/or the verification engineer needs to run their simulation only once after the bug has been detected.

The secondary run records all needed debug data needed for the user to isolate the bug. No need to run multiple sets of simulations to find the bug... A significant savings in debug time!

This tutorial will explain some simple techniques that the user can implement up front in their code that will allow for improved debug later in their project. We will also demonstrate how you can quickly step forward or backward through your source code in a post process debug environment, or click on any line or variable directly to get to the point in time when the line executed or variable changed. And we will also show you how you can seamlessly navigate from HDL to HVL code when exploring the root cause of issues.

The tutorial session will also cover topics including:

• UVM debug
• Low-power debug
• RTL debug
• X-propagation support
• Performance improvements [tips and tricks]

Speakers:
Nadav Chazan - Cadence Design Systems, Inc.
Corey Goss - Cadence Design Systems, Inc.
Kishore Karnane - Cadence Design Systems, Inc.
Thursday, March 6

**Tutorial 11 - Formal Verification in Practice: Technology, Methods and Applications**

**Siskiyou Ballroom**

**2:00 - 5:30pm**

**Organizer:**

**Rebecca Granquist** - Mentor Graphics Corp.

Across the industry today, the effort spent on verification continues to grow at an alarming pace. At the same time, time-to-market is one of the major constraints for project teams. As designs are always increasing in size and complexity, so is the need to verify with higher efficiency in order to stay competitive. However, there are some specific problem areas that arise over the course of the verification process that introduce bottlenecks and act as barriers to improving the efficiency. Many of these problem areas can be tackled with formal-based technologies which help to improve design quality and predictably shorten the schedule.

Attendees of this tutorial will learn how formal-based technologies are boosting verification efficiency in multiple domains. The session will include a review of the technology and methods behind these solutions, and will include users sharing their experiences in the application of formal to overcome a variety of verification challenges.

The tutorial will cover:

- Fully automatic formal solutions for
  - Clock domain crossings
  - RTL design checks
  - X-state verification
  - Property generation
  - Coverage closure

- Automated formal apps for verification of
  - Design constraints
  - Connectivity
  - Register access

- Property checking
  - Formal engines
  - Using Non-determinism
  - Data independence

Our guest speakers for this tutorial include:

- Nguyen Le from Microsoft, who will present a case study of using formal for code coverage closure
- Paul Egan and Kathleen Otten from Rockwell Automation, presenting on the way they used formal, including connectivity checking, to meet regulatory requirements for safety
- Ram Narayan from Oracle Labs, who will describe the experience of using formal property checking for verification of portions of a large SoC
- Vigyan Singhal from Oski Technologies, presenting on the topic of formal verification of cache coherency with the ARM ACE/CHI protocols

**Speakers:**

- **Mark Eslinger** - Mentor Graphics Corp.
- **Ram Narayan** - Oracle Labs
- **Jeremy Levitt** - Mentor Graphics Corp.
- **Nguyen Le** - Microsoft Corp.
- **Paul Egan** - Rockwell Automation, Inc.
- **Kathleen Otten** - Rockwell Automation, Inc.
- **Vigyan Singhal** - Oski Technology, Inc.

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Time-to-market pressure continues to increase in the semiconductor industry, and verification teams are rarely given the amount of time required to completely validate all aspects of a design. Structural and functional coverage are essential metrics to ensure that a design has been tested enough, but even achieving 100% coverage does not mean a design is thoroughly tested. Coverage metrics assume that the cases being tested for are comprehensive and rely on engineers to add random or directed stimulus to cover missing scenarios.

There are many issues with these assumptions:

1. Code coverage only speaks about whether a structure was activated, but not if its results were propagated and detected by the verification environment;
2. Functional coverage is subjective, hand generated and often incomplete;
3. Writing and running thousands of random tests with multiple seeds to close coverage is an inefficient use of hardware and engineer resources;
4. Coverage closure requires time-consuming analysis to identify unreachable coverage goals, understand whether they are design bugs, testbench flaws, or truly unreachable; and
5. When there are valid unreachable goals, the process of generating and maintaining waivers for those cases is time consuming.

This tutorial details a methodology for ensuring that the verification environment itself is complete, identifying unreachable functional and structural points, and automating the process of closing coverage and generating waivers for unreachable code to help drive coverage closure quickly and efficiently. We explain the methodology structure, methods for reducing coverage analysis time, and techniques to automate the generation of high quality tests, waivers, and checkers.

Speaker:
Alex Wakefield - Synopsys, Inc.
RTC magazine spotlights trends and breakthroughs in the design, development and technology of embedded computers. RTCMAGAZINE.COM

MEDS cooperates with leading medical device manufacturers and community groups to educate and promote the best practices for medical device manufacturers and developers through a series of events and magazines. MEDSMAGAZINE.COM

COTS Journal provides the industry with the best quality technical material to help readers design and build embedded computers for the military. COTSGONLINE.COM

Intelligent Systems Source is a parametric search engine for design engineers seeking a side-by-side comparison of off-the-shelf system modules and SBCs. Join our monthly Intelligent Systems Source e-newsletter and be informed on the latest boards and modules. Have access to informational articles and whitepapers involving the intelligent systems industry. INTELLIGHTENTSYSETMSSOURCE.COM

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**Monday, March 3 - 5:00 - 7:00pm - 1st Annual Booth Crawl!**

**Tuesday, March 4 - Wednesday, March 5 - 2:30 - 6:00pm**

Bayshore Ballroom

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1005

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